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Battery charger/discharger for bipolar microgrids with synchronous bus voltage regulation

Cargador/descargador de baterías para microrredes bipolares con regulación sincrónica de voltaje

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Abstract:

Bipolar DC microgrids offer significant advantages in power distribution and are particularly useful for isolated applications. This paper proposes and designs a battery charger/discharger adapted explicitly for these systems, addressing the challenge of generating the bipolar bus from a single battery, which is crucial capability for isolated microgrids. The work focuses on the synchronous regulation of both positive and negative DC bus voltages $(v_p = v_n)$ using a robust sliding-mode control (SMC) strategy. The converter's power stage, in a half-bridge configuration, is designed for this synchronous regulation. The chosen SMC provides global stability and robustness for these non-linear switching converters. A systematic design procedure is detailed for critical converter parameters, including the inductor, bus capacitances, weighting factor, and hysteresis band, ensuring desired performance in terms of voltage deviation, settling time, and switching frequency. Circuital simulations, performed in PSIM, rigorously verify the correct operation and robust voltage regulation under diverse operational scenarios, including unbalanced and balanced current consumption and production. The proposed approach was tested in a particular application example, which confirms the precise bus voltage regulation within specified limits (24 V 2.5%), achieving desired settling times (0.1 ms at 1% band), and verifying the correct limitation of the switching frequency (below of 100 kHz), thus validating the proposed design and control approach.

Keywords: battery charger/discharger; synchronous bipolar DC microgrid; sliding-mode control; integrated design process; bus capacitance.

Resumen:

Las microrredes DC bipolares ofrecen ventajas significativas en la distribución de energía y son particularmente útiles para aplicaciones aisladas. Este artículo propone y diseña un cargador/descargador de baterías específicamente adaptado para estos sistemas, abordando el desafío de generar el bus bipolar a partir de una única batería, la cual es una capacidad crucial para las microrredes aisladas. El trabajo se centra en la regulación síncrona de los voltajes del bus DC bipolar $(v_p = v_n)$ mediante una estrategia de control por modos deslizantes (SMC). La etapa de potencia del convertidor, en configuración de medio puente, está diseñada para esta regulación síncrona. El SMC elegido proporciona estabilidad global y robustez en estos convertidores conmutados no lineales. Se detalla un procedimiento de diseño sistemático para los parámetros críticos del convertidor, incluyendo el inductor, las capacitancias del bus, el factor de ponderación y la banda de histéresis, asegurando así el rendimiento deseado en términos de desviación de voltaje, tiempo de establecimiento y frecuencia de conmutación. Simulaciones circuitales, realizadas en PSIM, verifican rigurosamente el funcionamiento correcto y la regulación robusta de voltaje bajo diversos escenarios operativos, que incluyen consumo y producción de corriente desequilibrados y equilibrados. La solución propuesta se evaluó usando un ejemplo de aplicación, lo que confirmó la regulación precisa de voltaje dentro de los limites definidos (24 V ± 2.5%), logrando los tiempos de establecimiento requeridos (0.1 ms en una banda de 1%), y verificando la limitación de la frecuencia de conmutación (menor a 100 kHz), lo que valida el procedimiento propuesto para diseño y control del sistema.

Palabras clave: cargador/descargador de batería; microrred bipolar DC síncrona; control por modos deslizantes; proceso de diseño integrado; capacitancia del bus.

INTRODUCTION

DC microgrids are currently an alternative for electrical energy distribution, and they are useful in isolated environments together with distributed generation. A bipolar microgrid is a DC microgrid architecture that offers advantages over the unipolar architecture. The main advantages include greater flexibility in the voltage level thanks to its unipolar and bipolar operation, higher efficiency due to the reduction of current in the conductors, greater service continuity thanks to the presence of three terminals (neutral, negative and positive poles), integration of various renewable energy sources with different voltage levels, and smaller size and cost of the converters due to operation at high voltages[1].

A bipolar DC bus is frequently obtained using a three-phase AC/DC converter, where the systems are connected to an AC grid [2], [3]. A rectifier converts the three-phase voltage and splits it into two buses using a neutral point, thus generating the +Vdc/2 and -Vdc/2 levels. When the systems operate in isolation, however, they can take advantage of the bipolar microgrid architecture. Generating a bipolar bus from a single battery creates an isolated DC microgrid, with the bipolar bus produced from a single energy source. In this case, a bipolar DC/DC converter is used to connect the source and the loads, regulating the voltage at both poles. This structure is useful for supplying power to rural communities or mobile applications, since it reduces the number of power sources required, facilitates energy balance between the poles, and maintains voltage levels even with unbalanced loads [4].

In contrast to the advantages offered by bipolar microgrids, their correct operation presents technical requirements. For example, when the loads connected to the +Vdc/2 and –Vdc/2 poles have different values, a voltage imbalance occurs. This imbalance can be resolved by means of a voltage balancer, which maintains a stable midpoint and regulates the difference between the positive and negative pole voltages. The balancer redistributes the energy between the poles, maintaining $V+ \approx V-$. The control of these systems involves the regulation of two output voltages that share a common midpoint, which means that load variations in one pole directly affect the other[5]. This introduces a phenomenon known as cross-coupling in the system dynamics, which cannot be mitigated by independent linear controllers that do not guarantee a stable and balanced behavior[2],[6],[7],[8],[9]. This is the case of[2], where linear controllers (double-integrator lead structures) are used to regulate each branch. Because these controllers are designed at a particular operating point, global stability and unified performance cannot be guaranteed. Conversely, the solution reported in [6] presents a controller designed with an averaged model, which limits the frequency response of the system. In addition, that solution uses a controller based on backstepping, requiring the tuning of two parameters using particle swarm optimization, which implies slow training for each application. The work reported in [7] is also based on two first-order linear controllers (washout filters) tuned at the nominal operating point, which prevents guaranteeing global performance. Likewise, that control technique includes low-pass filters to remove high-frequency transients, which introduces delays in the dynamic response of the voltage regulation. A different limitation is observed in[8], where the entire control system is based on a small-signal model. This implies that any control design is limited to a particular operating point, which prevents guaranteeing global stability. Finally, the work reported in [9] makes evident the need for controllers with global stability and performance. That work reports multiple operating scenarios for bipolar DC buses, where the battery charger/discharger must withstand very different operating conditions; therefore, locally stable (or small-signal) controllers cannot ensure the desired system performance.

A sliding mode controller (SMC) can consider the interaction between the two poles and preserve their symmetry. This control technique is appropriate for the regulation of power converters due to its robustness against variations in inductance, resistance, loads and/or sources. In addition, an SMC strategy provides global stability in nonlinear systems thanks to its sliding surface; this makes it ideal for operating with e.g. battery charger/discharger converters[10],[11].

The main contribution of this article is the design of an advanced strategy to control the two branches of a bipolar microgrid, using an SMC that simultaneously regulates both voltages, thus ensuring global stability and the performance of both branches. This is achieved with a sliding surface that combines the errors of both voltages into a single switching function. In this way, the SMC produces a single action on the converter to regulate the voltages at the two poles. In contrast to other solutions based on two controllers (one for each branch), the use of a single controller reduces system complexity and ensures a dynamic balance between the branches, even under unbalanced conditions and with fast power variations. In addition, the SMC is designed with the nonlinear switched model, which avoids bandwidth penalties caused by averaging or small-signal approximations. To provide a complete solution, the design of the power stage using a half-bridge configuration is also discussed. Finally, simple design equations are provided, which avoids slow training processes for the controller. This comprehensive procedure for the design and control of the battery charger/discharger ensures the maximum desired voltage deviation, settling time, and maximum switching frequency.

The rest of the article is organized as follows: Section 2 presents the power stage of the battery charger/discharger and its model; Section 3 includes the complete design of the sliding-mode controller; and Section 4 presents the design and estimation of the bus capacitances. Section 5 includes a design procedure and an application example. Finally, a circuit simulation is carried out to validate the design of the battery charger/discharger elements and the SMC parameters.

POWER STAGE OF THE BATTERY CHARGER/DISCHARGER

The proposed battery charger/discharger for bipolar DC microgrids is described in Fig. 1. The power stage consists of two MOSFETs in half-bridge configuration, where the upper MOSFET is switched on with the control signal u, while the lower MOSFET is switched on with $\overline{u}$ = 1 - u. The circuit has two capacitors, C_p and C_n, also in half-bridge configuration, which are used to regulate the voltages of the bipolar buses v_p and v_n. This solution is designed for synchronous bipolar buses, that is, $v_p = v_n$. Finally, an inductor L is used to charge and discharge the capacitors, which enables regulation of the bipolar DC bus. Since the power stage is designed for synchronous bipolar DC buses, the capacitors are selected equal ($C_p = C_n$) to withstand the same maximum current in each branch, i.e. positive and negative.

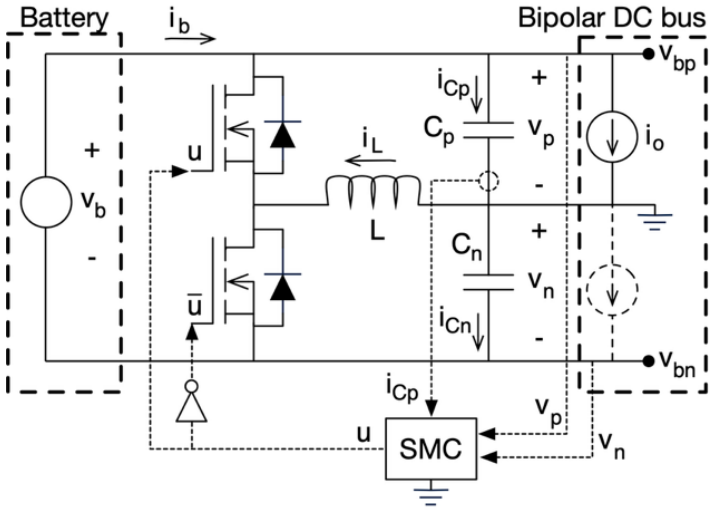

Fig. 1. *Battery charger/discharger for a synchronous bipolar bus.*
Source: own elaboration.

The switched model of this power stage is obtained by calculating the differential equations of the inductor current and the capacitor voltages through the charge and volt-second balance principles[12]. These differential equations are then combined considering each value of the control signal (u = 1 and u = 0), as shown in (1) and(2). In addition, (3) represents the battery current and (4) models the magnitude of the negative bus voltage.

$$\frac{d\,i_L}{dt} = \frac{v_b \bullet \overline{u} - v_p}{L} \quad (1)$$

$$\frac{d\,v_p}{dt} = \frac{i_L - i_o}{2 \bullet C_p} \quad (2)$$

$$i_b = \frac{(1 - 2 \bullet u) \bullet i_L + i_o}{2} \quad (3)$$

$$v_n = v_b - v_p \quad (4)$$

Considering that the duty cycle of the converter is the average value of the control signal, i.e. $d = (1/T) \bullet \int_0^T u\,dt$, then the averaged model is:

$$\frac{d\,i_L}{dt} = \frac{v_b \bullet (1 - d) - v_p}{L} \quad (5)$$

$$\frac{d\,v_p}{dt} = \frac{i_L - i_o}{2 \bullet C_p} \quad (6)$$

$$i_b = \frac{(1 - 2 \bullet d) \bullet i_L + i_o}{2} \quad (7)$$

$$v_n = v_b - v_p \quad (8)$$

Finally, the stable conditions of the power stage are obtained by considering the derivatives equal to zero:

$$v_n = v_b \bullet (1 - d) \quad (9)$$

$$i_L = i_o \quad (10)$$

SLIDING-MODE CONTROLLER

The proposed control system is based on sliding-mode control theory (SMC), which can provide global stability to non-linear switched converters [10], [11]. The first step is to design the switching function s_x of the sliding-mode controller. Since the main control objective is to regulate a synchronous bipolar DC bus, the magnitude of the positive and negative voltages must be equal. Therefore, the term $k(v_P - v_n)$ is defined as a component of s_x, where k is a weighting factor that will be calculated later. Additionally, to provide a fast dynamic response, the current i_{Cp} of C_P is also defined as a component of s_x, so changes in the current bus are detected without delay since $i_{Cp}=(i_L - i_o)/2$ as reported in (2). The combination of both components results in the following switching function s_x and in the sliding surface S_U:

$$s_x = i_{Cp} + k \bullet (v_p - v_n) \tag{11}$$

$$S_U = \{s_x = 0\} \tag{12}$$

The slip surface (12) ensures both zero error and stability: it ensures equal voltage magnitudes on the bus branches, and ensures stable voltages on the bus. Fig. 1 shows the interaction of the SMC with the power stage. Finally, the analysis of the overall stability of this SMC requires cross-sectionality and reachability tests $v_p - v_n = 0 i_{Cp} = 0$ 13, las cuales se describen a continuación.

Transversality Analysis

The transversality analysis evaluates the ability of the SMC to control the system trajectory. Therefore, this analysis verifies the presence of the control signal in the derivative of the switching function, which is reported in(13). The formalization of this transversality analysis is presented in (14). Then, evaluating (14) in (13) results in (15), which confirms the transversality condition.

$$\frac{d\,s_x}{dt} = \frac{v_b \bullet \overline{u} - v_p}{2 \bullet L} - \frac{1}{2} \bullet \frac{d\,i_o}{dt} + \frac{i_L - i_o}{C_p} \tag{13}$$

$$\frac{d}{du}\left(\frac{d\,s_x}{dt}\right) \neq 0 \tag{14}$$

$$\frac{d}{du}\left(\frac{d\,s_x}{dt}\right) = -\frac{v_b}{2 \bullet L} < 0 \tag{15}$$

Reachability analysis

The reachability test verifies the ability of the SMC to reach the desired sliding surface $S_U = \{s_x = 0\}$. This condition requires changing the derivative of the switching function in the direction of the surface: positive derivative if $s_x < 0$ and negative derivative if $s_x > 0$. That action depends on the sign of the transversality (15), which is negative; thus, $u = 1$ produces a negative derivative and $u = 0$ produces a positive derivative. These conditions are formalized below:

$$\lim_{s_x \to 0^-} \frac{d\,s_x}{dt}\Big|_{u=0} > 0 \quad , \quad \lim_{s_x \to 0^+} \frac{d\,s_x}{dt}\Big|_{u=1} < 0 \tag{16}$$

The evaluation of the above expressions, using (13), produces the inductor constraint reported in (17). That expression describes the maximum inductor value that ensures global stability, which depends on the desired voltage v_p and the maximum derivative of the load current in the bus branches. Therefore, the inductor L must be designed following (17) to ensure reachability. Finally, compliance with the reachability and transversality conditions ensures the global stability of the SMC [13].

$$L < \frac{v_p}{\left|\frac{d\,i_o}{dt}\right|} \tag{17}$$

Equivalent dynamics

The weighting factor k is calculated to impose a desired stabilization time on the bus voltage after a load current transient. This calculation assumes correct operation of the SMC, which is ensured by the global stability discussed in Subsections 3.1 and 3.2. Global stability likewise ensures operation within the sliding surface (12), i.e. $S_U = \{s_x = 0\}$. The SMC therefore imposes $i_{Cp} = -k \bullet (v_p - v_n)$, and substituting (6) and (9) yields the equivalent closed-loop dynamics for the bus voltage. Since the desired operating condition is $v_p = v_n = v_b/2$, the resulting time-domain expression (18) follows from $v_p - v_n = 2 \bullet v_p - v_b$. Then (18) is transformed to the Laplace domain as shown in (19), relating the voltage perturbations in the positive bus v_p to the desired condition $v_b/2$.

$$C_p \bullet \frac{d\,v_p}{dt} = -k \bullet (2 \bullet v_p - v_b) \tag{18}$$

$$G_{CL} = \frac{\widehat{v_p}}{(\widehat{v_b}/2)} = \frac{1}{\left(\frac{C_p}{2 \bullet k}\right) \bullet s + 1} \quad 19$$

The design of k targets the worst-case scenario, which considers a step change in the bus voltage equal to the maximum allowed deviation Δv_p. In the Laplace domain, that perturbation is formalized as $\widehat{v_b}/2 = \frac{\Delta v_p}{s}$. The dynamic behavior of the bus voltage is then calculated as $\widehat{v_p} = G_{CL} \bullet \frac{\Delta v_p}{s}$, which gives the time-domain expression for the bus voltage in (20). The stabilization time is measured when the bus voltage enters a safe band ϵ, i.e. $\widehat{v_p} = \epsilon \bullet v_b/2$, where the voltage required for compensation is $\Delta v_p - \epsilon \bullet v_b/2$. Substituting that value in (20) gives the design expression for k reported in (21), which ensures the desired stabilization time for the bus voltage.

$$\widehat{v_p} = \Delta v_p \bullet \left(1 - e^{-t/\left(\frac{C_p}{2 \bullet k}\right)}\right) \quad 20$$

$$k = \frac{-\ln\left(\frac{\epsilon \bullet v_b/2}{\Delta v_p}\right) \bullet C_p}{2 \bullet t_s} \quad 21$$

Switching frequency

The theoretical sliding surface reported in (12) could introduce very high switching frequencies near $s_x = 0$. This problem is addressed by introducing a hysteresis band around the surface [13], which limits the maximum switching frequency F. This limitation is formalized in (22), where H is the hysteresis band.

$$S_{UP} = \{s_x \leq H\} \quad 22$$

The surface in (22) imposes a ripple in the switching function equal to H. That ripple is calculated from (11) as $H = \Delta i_L/2$, where Δi_L is the inductor current ripple. Δi_L is divided by 2 because half of the inductor current is processed in capacitor C_P as reported in (2), i.e. $i_{Cp} = i_L/2$. The inductor current ripple is then calculated from (1) as $\Delta i_L = v_p \bullet d \bullet T/(2 \bullet L)$. From (9), a duty cycle $d = 0.5$ is also calculated for the desired operating condition $v_p = v_n = v_b/2$. Based on the previous analysis, expression (23) is obtained for the hysteresis band H, which ensures a maximum switching frequency F.

$$H = \frac{v_p}{8 \bullet L \bullet F} \quad 23$$

DESIGN OF THE BUS CAPACITANCES

The bus capacitors $C_P = C_n$ are sized to limit the bus voltage deviation caused by the maximum current disturbance Δi_o allowed in the bipolar bus. This calculation requires the analysis of the voltage and current waveforms in the capacitor C_P. Fig. 2 shows the ground node of the bipolar charger/discharger, and the analysis considers a step change in the bus current Δi_o, which corresponds to the worst-case scenario. The waveform of the output current i_o exhibits a downward step disturbance with magnitude Δi_o, which is compensated by the SMC with a decrease in the current i_{Cp} of the capacitor C_P. However, expression (2) reports that the current in the capacitor depends on half of the output current i_o and half of the inductor current i_L, so the step of the load current Δi_o is instantaneously transferred to i_{Cp} divided by 2. In contrast, the inductor current can change with the maximum slope defined in (1), and its effect is transferred to i_{Cp} divided by 2 during a time interval ΔT_Q. Fig. 2 shows the waveforms of i_o, i_L and i_{Cp}.

The interval ΔT_Q is the time required by i_{Cp} to reach 0 starting from $\Delta i_o/2$, resulting in expression (24). That expression is based on the derivative of the inductor current reported in (1) for $u = 1$.

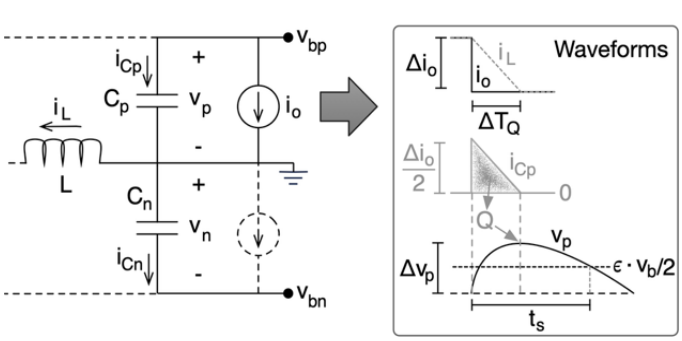

Fig. 2. *Analysis of the voltage deviation in the bus.*
Source: own elaboration.

$$\Delta T_Q = \frac{\Delta i_o/2}{\frac{1}{2} \bullet \frac{d\,i_L}{dt}} = \frac{2 \bullet L \bullet \Delta i_o}{v_b} \quad (24)$$

The waveform of i_{Cp} shows that a positive charge Q is stored in the capacitor C_P during the transient. That charge is calculated as the area of the triangle formed by $\Delta i_o/2$ and ΔT_Q, resulting in $Q = \Delta T_Q \bullet \Delta i_o/4$. The waveform in the middle of Fig. 2 illustrates this concept. In addition, that positive charge produces an increase in the voltage v_p of the capacitor C_P defined by $\Delta v_p = Q/C_P$. Finally, by operating the previous expressions, including (24), the calculation of C_P that ensures a maximum deviation Δv_p is reached:

$$C_P = \frac{L \bullet {\Delta i_o}^2}{2 \bullet v_b \bullet \Delta v_p} \quad (25)$$

DESIGN PROCEDURE AND APPLICATION EXAMPLE

This section synthesizes the design process, which is illustrated with an application example.

Synthesis of the design process

The first step is to define the application requirements: battery voltage (v_b), synchronous bipolar voltages ($v_p = v_n = v_b/2$), maximum current derivative in the buses $\left|\frac{d\,i_o}{dt}\right|$, maximum amplitude of the load current disturbances (Δi_o), maximum voltage deviation in the buses (Δv_p), settling time (t_s) for a safe band (ϵ), and a maximum switching frequency supported by the components (F).

Then the inductor L is calculated with (17) to ensure global stability. The third step is to calculate the bus capacitors $C_P = C_n$ with (25), an equation that limits the bus voltage deviations to Δv_p. The fourth step is to calculate the weighting factor k from (21) to ensure the desired settling time t_s. Finally, the hysteresis band of the SMC is calculated from (23) to limit the switching frequency to F.

Application example

This application example considers a battery voltage $v_b = 48\ V$, which is used to support the synchronous bipolar bus by delivering $24\ V$ to the branches ($v_p = v_n = 24\ V$). In this example, the sources and loads connected to the bus impose a maximum current derivative $\left|\frac{d\,i_o}{dt}\right| = 100\ A/ms$, with a maximum amplitude of the current disturbances $\Delta i_o = 2\ A$. In addition, correct operation of these sources and loads requires limiting the voltage deviations of the branches to $2.5\ \%$; therefore, a maximum deviation of $0.6\ V$ must be ensured. The loads and sources of this example withstand a voltage deviation for $t_s = 0.1\ ms$ for a band of $\epsilon = 1\%\ (0.24\ V)$ in the bus. Finally, the devices used in the construction of the converter withstand a maximum switching frequency $F = 100\ kHz$. These requirements are summarized in Table 1.

Following the design procedure of Subsection 5.1, a maximum inductance of the converter of $240\ \mu H$ is calculated with (17), selecting a commercial inductance $L = 200\ \mu H$. The minimum bus capacitances are calculated as $13.72\ \mu F$ from (25), selecting the commercial capacitors $C_P = C_n = 15\ \mu F$. The weighting factor $k = 0.07\ A/V$ is then calculated using (21). Finally, the hysteresis band $H = 0.15\ A$ is calculated with (23). Table 2 summarizes the parameters of the bipolar charger/discharger.

Table 1: Requirements for the application example

Requirement	Value
v_b	48 V
$v_p = v_n$	24 V
$\left\|\frac{d\,i_o}{dt}\right\|$	100 A/ms
Δi_o	2 A
Δv_p	2.5 % (0.6 V)
t_s	0.1 ms
ϵ	1% (0.24 V)
F	100 kHz

Source: own elaboration.

Table 2: Parameters of the bipolar charger/discharger

Parameters	Value
L	μH 200
$C_p = C_n$	$15\ \mu F$
k	$0.07\ A/V$
H	0.15 A

Source: own elaboration.

CIRCUITAL SIMULATIONS

The previous design example is verified using detailed circuital simulations performed in the professional power electronics simulator PSIM® 2022. The simulator was configured with an integration time of 10 ns, and the MOSFET model includes an ON resistance of 4.8 m, a diode forward voltage of 3 V, and a resistance of 1 m for the parasitic diode.

Subsequently, the circuital schematic of Fig. 1 was implemented in PSIM using the parameters of Table 2. Fig. 3 shows the PSIM circuit, where the negative bus voltage is measured at the lowest node, so this is the negative value of the bus voltage magnitude. This is compensated by adding both bus voltages, positive and negative, to form the $k \bullet (v_p - v_n)$ component of the s_x function (11).

Additionally, Fig. 3 also shows the hysteresis comparator implementing the practical sliding surface $S_{UP} = \{s_x \leq H\}$ previously defined in (22). This hysteresis comparator is formed by two classic comparators and an S-R flip-flop, which produces the control signal u of the MOSFETs.

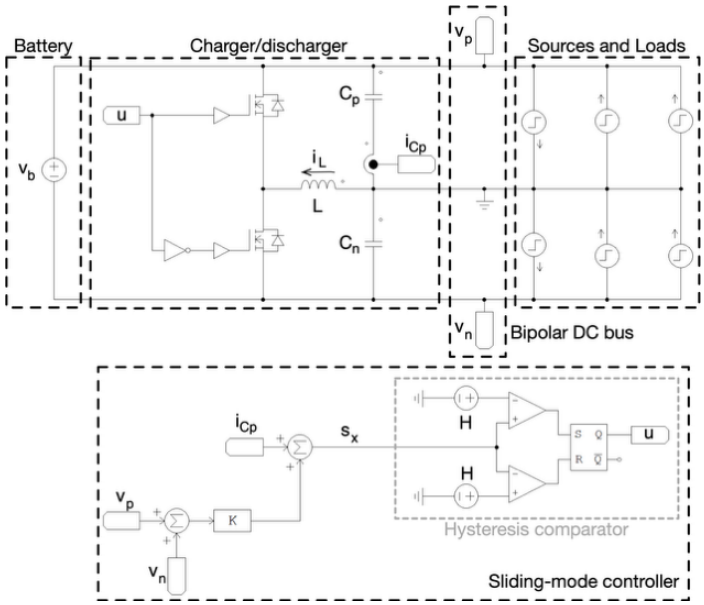

Fig. 3. *PSIM implementation of the bipolar charger/discharger.*
Source: own elaboration.

The simulation circuit of Fig. 3 considers six current changes in both buses, the positive and the negative. Fig. 4 reports the simulation results, where at 0.5 ms the positive bus has a current consumption of 1 A, which produces an unbalanced consumption from the standby negative bus (0 A). Under that condition both buses are perturbed, but their regulation is correct; the voltage deviation in this case is small (0.8 %) because the current perturbation is lower than the Δi_o defined in Table 1, fulfilling the deviation requirement (lower than 2.5 %). At 1.5 ms the negative bus has a current perturbation of 2 A (equal to Δi_o in Table 1), producing an unbalanced consumption. Again, both bus voltages are perturbed and correctly regulated with a deviation of 1.9 % < 2.5 %. At 2.5 ms the current consumption in the negative bus is reduced to 1 A, which produces a balanced current consumption; again, both buses are correctly regulated with a voltage deviation of 0.5 % < 2.5 %.

At 3.5 ms the current in the positive bus becomes negative (-1 A), which is taken to mean that a source is producing energy. Current consumption in the negative bus and current production in the positive bus therefore occur at the same time. As in the previous case, both bus voltages are correctly regulated, here with a deviation of 1.7 % < 2.5 %. At 4.5 ms the current in the negative bus becomes negative, which implies that a source in that bus is also producing energy. This produces a balanced production in both buses (-1 A), where $\Delta i_o = 2\ A$, as defined in Table 1. In this case, both bus voltages are correctly regulated with a deviation of 2.2 % < 2.5 %. Finally, at 5.5 ms the production in the positive bus increases (-2 A), producing an unbalanced production in the bipolar DC bus. As in the previous cases, both bus voltages are correctly regulated, here with a deviation of 0.4 % < 2.5 %.

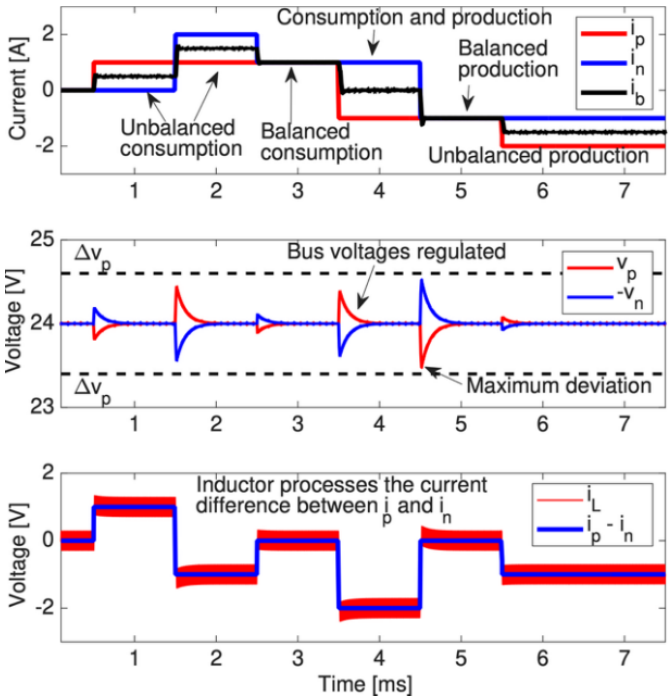

Fig. 4. *Circuital simulation.*
Source: own elaboration.

In conclusion, the circuit simulation of Fig. 4 confirms the correct regulation of the bipolar DC bus under any operating condition. The battery current is also observed to be always the average value of the current in both buses. This is expected, since the current production in one bus can be used to supply the current consumption in the other bus. This is confirmed in the waveforms at the bottom, where the inductor current only processes the difference between the currents in the buses.

Fig. 5 shows a zoom between 4.46 ms and 4.70 ms, which corresponds to a transient $\Delta i_o = -2\ A$ in the negative bus. The figure confirms the correct design of both the converter and the controller: the bus voltage deviation is always below the limit $\Delta v_p = 0.6\ V$ (0.53 V or 2.2 % < 2.5 %), and the stabilization time is equal to $t_s = 0.1\ ms$ for a band of $\epsilon = 1\ \%\ (0.24\ V)$. Finally, the switching frequency, measured in i_L, is equal to 100 kHz. In conclusion, the proposed design procedure (whose result is the parameters of Table 2) provides the desired operating characteristics defined in Table 1.

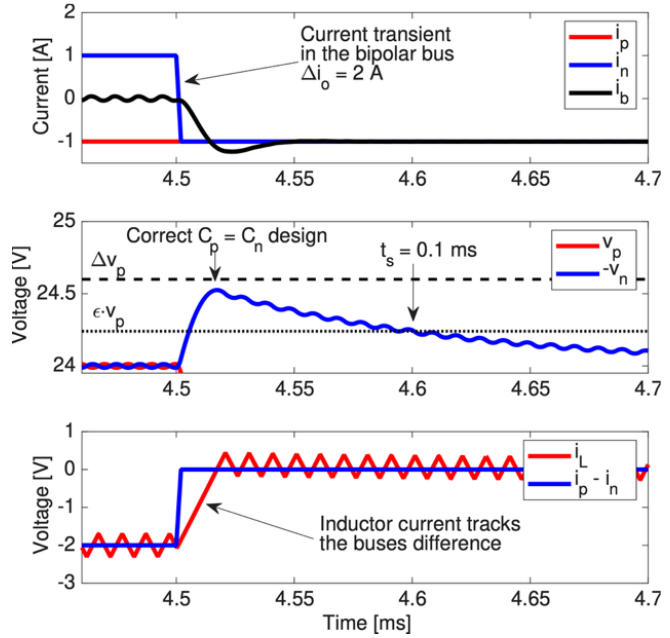

Fig. 5. *Verification of the stabilization time and the maximum deviation.*
Source: own elaboration.

CONCLUSIONS AND FUTURE WORK

This work successfully proposed, designed and verified a battery charger/discharger system explicitly dedicated to synchronous bipolar DC microgrids. The core of the system is the sliding-mode control strategy, which effectively regulates the bipolar bus voltages and ensures that the positive (v_p) and negative (v_n) poles remain equal in magnitude and stability. The global stability of the nonlinear controller was rigorously confirmed through the transversality and reachability analyses, showing its robustness for switched-converter applications. A significant contribution of this research is the establishment of a systematic and rigorous design procedure that enables the calculation of the critical parameters, including the inductor (L), the bus capacitors (C_p, C_n), the weight factor of the sliding surface (k), and the hysteresis band (H). These calculations are based on application requirements such as the maximum voltage deviation, the stabilization time and the maximum switching frequency.

The performance of the converter and its controller was validated through circuital simulations in PSIM under multiple operation scenarios, including balanced and unbalanced conditions of current absorption and delivery. The results confirm a voltage regulation that meets all the desired operation characteristics. In addition, the system handles power flow efficiently, allowing current production in one bus to supply the consumption in the other bus. This is confirmed in the simulation of the battery current, which corresponds to the average of the currents in the two buses.

Based on these results, several lines of future work are proposed. The most immediate step is to validate the solution experimentally in a physical prototype, confirming the theoretical and simulation results under real conditions, including the non-idealities and tolerance of the components. The research could then focus on improving the fault tolerance of the system by analyzing its behavior during anomalous conditions such as short circuits, an open circuit in a branch of a bipolar microgrid, or extreme load transients. Finally, while current control ensures stability, another line of future work could explore optimization techniques to improve the efficiency and dynamic response of the entire system, investigate alternative modulation techniques, use wide-bandwidth converters, or develop adaptive control algorithms to minimize losses across a broader range of operating points.

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CONFLICT OF INTEREST

None

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