Battery charger/discharger for bipolar microgrids with synchronous bus voltage regulation

Cargador/descargador de baterías para microrredes bipolares con regulación sincrónica de voltaje

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Abstract: Bipolar DC microgrids offer significant advantages in power distribution and are particularly useful for isolated applications. This paper proposes and designs a battery charger/discharger adapted explicitly for these systems, addressing the challenge of generating the bipolar bus from a single battery, which is crucial capability for isolated microgrids. The work focuses on the synchronous regulation of both positive and negative DC bus voltages $(v_p = v_n)$ using a robust sliding-mode control (SMC) strategy. The converter's power stage, in a half-bridge configuration, is designed for this synchronous regulation. The chosen SMC provides global stability and robustness for these non-linear switching converters. A systematic design procedure is detailed for critical converter parameters, including the inductor, bus capacitances, weighting factor, and hysteresis band, ensuring desired performance in terms of voltage deviation, settling time, and switching frequency. Circuital simulations, performed in PSIM, rigorously verify the correct operation and robust voltage regulation under diverse operational scenarios, including unbalanced and balanced current consumption and production. The proposed approach was tested in a particular application example, which confirms the precise bus voltage regulation within specified limits (24 V ± 2.5%), achieving desired settling times (0.1 ms at 1% band), and verifying the correct limitation of the switching frequency (below of 100 kHz), thus validating the proposed design and control approach.

Keywords: battery charger/discharger; synchronous bipolar DC microgrid; sliding-mode control; integrated design process; bus capacitance.

Resumen: Las microrredes DC bipolares ofrecen ventajas significativas en la distribución de energía y son particularmente útiles para aplicaciones aisladas. Este artículo propone y diseña un cargador/descargador de baterías específicamente adaptado para estos sistemas, abordando el desafío de generar el bus bipolar a partir de una única batería, la cual es una capacidad crucial para las microrredes aisladas. El trabajo se centra en la regulación

síncrona de los voltajes del bus DC bipolar $(v_p = v_n)$ mediante una estrategia de control por modos deslizantes (SMC). La etapa de potencia del convertidor, en configuración de medio puente, está diseñada para esta regulación síncrona. El SMC elegido proporciona estabilidad global y robustez en estos convertidores conmutados no lineales. Se detalla un procedimiento de diseño sistemático para los parámetros críticos del convertidor, incluyendo el inductor, las capacitancias del bus, el factor de ponderación y la banda de histéresis, asegurando así el rendimiento deseado en términos de desviación de voltaje, tiempo de establecimiento y frecuencia de conmutación. Simulaciones circuitales, realizadas en PSIM, verifican rigurosamente el funcionamiento correcto y la regulación robusta de voltaje bajo diversos escenarios operativos, que incluyen consumo y producción de corriente desequilibrados y equilibrados. La solución propuesta se evaluó usando un ejemplo de aplicación, lo que confirmó la regulación precisa de voltaje dentro de los limites definidos (24 V ± 2.5%), logrando los tiempos de establecimiento requeridos (0.1 ms en una banda de 1%), y verificando la limitación de la frecuencia de conmutación (menor a 100 kHz), lo que valida el procedimiento propuesto para diseño y control del sistema.

Palabras clave: cargador/descargador de batería; microrred bipolar DC síncrona; control por modos deslizantes; proceso de diseño integrado; capacitancia del bus.

1. INTRODUCTION

Today, DC microgrids are an alternative to distribute electric power and are useful in isolated environments in conjunction with distributed generation. A bipolar microgrid is one architecture of DC microgrids; which offers advantages over the unipolar microgrid architecture; such as greater voltage level flexibility due to their unipolar and bipolar operation, increased efficiency due the reduction of current in conductors, service continuity due to the presence of three terminals (neutral, negative and positive poles), integration of diverse renewable energy sources with different voltage levels, and reduced size and cost of converters due the operation of high voltages [1].

A bipolar DC bus is frequently obtained through a three-phase AC/DC converter when systems are connected to an AC grid [2], [3]; a rectifier converts the three-phase voltage and then divides it into two buses using a neutral point, thus generating the +Vdc/2 and -Vdc/2 levels. On the other hand, when systems operate in isolation, they can take advantage of a bipolar microgrid structure. Producing a bipolar bus from a single battery creates an isolated DC microgrid, with the bipolar bus generated from a single energy source. In that case, a bipolar DC/DC converter is used to interface the source and loads and to regulate the voltage of both poles. This structure is useful to supply rural communities or mobile applications, reducing the number of power sources required, facilitating energy balancing between the poles, and maintaining voltage levels under unbalanced loads [4].

In contrast to the advantages offered by bipolar microgrids, there are technical requirements for their correct operation. For example, when the loads connected to the +Vdc/2 and –Vdc/2 poles are different, a voltage imbalance occurs. This imbalance can be resolved through a voltage balancer, which maintains a stable midpoint and regulates the difference between the positive and negative voltages. The balancer redistributes energy between the poles, maintaining V+ ≈ V−. Controlling this type of system involves regulating two output voltages that share a common midpoint, meaning that load variations on one bus directly affect the other [5]. This introduces a phenomenon known as cross-coupling into the system dynamics, which cannot be mitigated by independent linear controllers that cannot guaranteeing stable and balanced behavior [2], [6], [7], [8], [9]. This is the case of [2], where linear controllers (integral-double-lead structures) are used to regulate each branch. Since those controllers are designed in a particular operation point, no global stability or unified performance is ensured. Instead, the solution reported in [6] presents a control design based on an averaged model, which limits the frequency response of the system. Moreover, that solution uses a backstepping-based controller, which requires to tune two parameters using particle swarm optimization, thus a lengthy training process must be conducted for each application. The work reported in [7] is also based on two first-order linear controllers (washout filters) tuned at the nominal operation condition, thus no global performance can be ensured. In addition, the control technique involves a low-pass filters to remove high-frequency transients, which introduce delays in the

dynamic response of the voltage regulation. A different limitation is observed in [8], in which the whole control structure is based on a small-signal model. This implies that any control design is constrained at the designed operation point, which makes impossible to guarantee global stability. Finally, the work reported in [9] shows the need of globally stable controllers with global performance. That work reports multiple operation scenarios for a bipolar DC bus, where the battery charger/discharger must support very different conditions, thus locally stable (or small-signal) controllers cannot ensure the desired system performance.

A sliding-mode controller can consider the interaction between the two poles and preserve their symmetry. This control technique is appropriate for power converter control due to its robustness to variations in inductance, resistance, loads, and/or sources. Additionally, an SMC strategy provides overall stability in nonlinear systems thanks to its sliding surface, making it suitable for use in converters such as battery chargers/dischargers [10], [11].

The main contribution of this paper is the design of an advanced strategy to control the two branches of a bipolar microgrid using an SMC that simultaneously regulates both voltages, thus ensuring the global stability and performance of both branches. This is achieved with a composite sliding-surface that combines the errors of both voltages into a single switching function. In this way, the SMC generates a single action on the converter to regulate the voltages of both poles. In contrast with other solutions based on two controllers (one for each branch), the adoption of a single controller reduces system complexity and ensures dynamic balance between branches under unbalanced loads and rapid power variations. In addition, the proposed SMC is designed with the switched non-linear model, hence no bandwidth penalization is introduced due to averaging or small-signal approximations. To provide a complete solution, the design of the power stage, using a half-bridge configuration, is also discussed. Finally, simple design equations are provided, which avoids lengthy training processes for the controller. This comprehensive design and control procedure ensures the desired maximum voltage deviation, settling time, and maximum switching frequency.

The rest of the paper is organized as follows: Section 2 presents the power stage of the battery charger/discharger and its model. Section 3 includes a complete design of the sliding mode controller and Section 4 presents the design and estimation of the bus capacitances. A design procedure and an application example are included in Section 5. Finally, a circuital simulation is carried out to validate the design of the elements in the battery charger/discharger and the parameters of the SMC.

2. POWER STAGE OF THE BATTERY CHARGER/DISCHARGER

The proposed battery charger/discharger for bipolar DC buses is depicted in fig. 1. The power stage is formed by two MOSFETs in half-bridge configuration, where the upper MOSFET is activated with the control signal u, while the lower MOSFET is activated with $\bar{u} = 1 - u$. The circuit has two capacitors C_P and C_n in half-bridge configuration, which are used to regulate the bipolar bus voltages v_P and v_n. This solution is designed for synchronous bipolar buses, i.e. $v_P = v_n$. Finally, an inductor L is used to charge and discharge the capacitors, thus enabling the regulation of the bipolar DC bus.

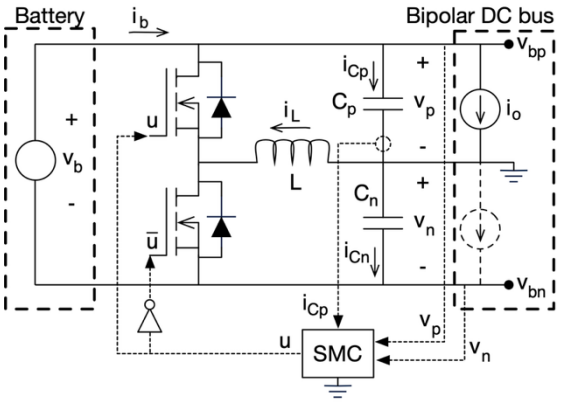

***Fig. 1**. Battery charger/discharger for bipolar synchronous bus.*
***Source:** own elaboration.*

Since the power stage is designed for synchronous bipolar DC buses, the capacitors are selected equal ($C_P = C_n$) to support the same maximum current in both positive and negative branches.

The switched model of this power stage is obtained by calculating the differential equations of the inductor current and capacitor voltages using the charge-balance and volt-second principles [12]. Then, those differential equations are combined considering each value of the control signal ($u = 1$ and $u = 0$) as given in (1) and (2). Moreover, (3) reports the battery current and (4) models the magnitude of the negative bus voltage.

$$\frac{d\,i_L}{dt} = \frac{v_b \cdot \bar{u} - v_p}{L} \quad (1)$$

$$\frac{d\,v_p}{dt} = \frac{i_L - i_o}{2 \cdot C_p} \quad (2)$$

$$i_b = \frac{(1-2\cdot u)\cdot i_L + i_o}{2} \quad (3)$$

$$v_n = v_b - v_p \quad (4)$$

Considering that the duty cycle of the converter is the average value of the control signal, i.e. $d = (1/T) \cdot \int_0^T u\,dt$, then the averaged model is:

$$\frac{d\,i_L}{dt} = \frac{v_b \cdot (1-d) - v_p}{L} \quad (5)$$

$$\frac{d\,v_p}{dt} = \frac{i_L - i_o}{2 \cdot C_p} \quad (6)$$

$$i_b = \frac{(1-2\cdot d)\cdot i_L + i_o}{2} \quad (7)$$

$$v_n = v_b - v_p \quad (8)$$

Finally, the stable conditions of the power stage are obtained considering the derivatives equal to zero:

$$v_n = v_b \cdot (1-d) \quad (9)$$

$$i_L = i_o \quad (10)$$

3. SLIDING-MODE CONTROLLER

The proposed control system is based on the sliding-mode control theory, which can provide global stability to non-linear switching converters [10], [11]. The first step is to design the switching function s_x of the sliding-mode controller. Since the main control objective is to regulate a synchronous bipolar DC bus, the magnitude of both positive and negative voltages must be equal. Therefore, the term $k(v_P - v_n)$ is considered as a component of s_x, where k is a weighting factor that will be calculated afterwards. In addition, to provide a fast dynamic response, the current i_{Cp} of C_P is also considered as a component of s_x, hence the changes on the bus current are detected without delay because i_{Cp}=$(i_L - i_o)/2$ as reported in (2). Combining both components results in the following switching function s_x and sliding surface S_U:

$$s_x = i_{Cp} + k \cdot (v_p - v_n) \quad (11)$$

$$S_U = \{s_x = 0\} \quad (12)$$

The previous sliding surface (12) ensures both null error and stability: $v_p - v_n = 0$ ensures equal voltages magnitudes in the bus branches, and $i_{Cp} = 0$ ensures stable bus voltages. Fig. 1 shows the interaction of the SMC with the power stage. Finally, the analysis of the global stability of this SMC requires both the transversality and reachability tests [13], which are described below.

3.1. Transversality analysis

The transversality analysis evaluates the SMC capability of controlling the system trajectory. Therefore, this analysis verifies the presence of the control signal into the switching function derivative, which is given in (13). The formalization of this transversality analysis is given in (14). Then, evaluating (14) using (13) results in (15), which confirms the transversality condition.

$$\frac{d\,s_x}{dt} = \frac{v_b \cdot \bar{u} - v_p}{2 \cdot L} - \frac{1}{2} \cdot \frac{d\,i_o}{dt} + \frac{i_L - i_o}{C_p} \quad (13)$$

$$\frac{d}{du}\left(\frac{d\,s_x}{dt}\right) \neq 0 \quad (14)$$

$$\frac{d}{du}\left(\frac{d\,s_x}{dt}\right) = -\frac{v_b}{2 \cdot L} < 0 \quad (15)$$

3.2. Reachability analysis

The reachability test verifies the SMC capability to reach the desired sliding surface $S_U = \{s_x = 0\}$. That condition requires to change the switching function derivative in the direction of the surface: positive derivative if $s_x < 0$ and negative derivative if $s_x > 0$. This action depends on the transversality sign (15), which is negative; thus, $u = 1$ produces a negative derivative and $u = 0$ produces a positive one. Those conditions are formalized as follows:

$$\lim_{s_x \to 0^-} \frac{d\,s_x}{dt}\bigg|_{u=0} > 0\,,\ \lim_{s_x \to 0^+} \frac{d\,s_x}{dt}\bigg|_{u=1} < 0 \quad (16)$$

Evaluating the previous expressions using (13) leads to the inductor restriction given in (17). Such an expression describes the maximum value of the inductor that ensures global stability. That limit depends on the desired v_p voltage and the maximum derivative of the load current in the bus branches. Hence, the inductor L must be designed following (17) to ensure the reachability. Finally, fulfilling reachability and transversality conditions ensure the global stability of the SMC [13].

$$L < \frac{v_p}{\left|\frac{d\,i_o}{dt}\right|} \quad (17)$$

3.3. Equivalent dynamics

The calculation of the weighting factor k is performed to impose the desired settling-time of the bus voltage after a load current transient. This calculation considers the correct operation of the SMC, which is ensured by the global stability

discussed in Subsections 3.1 and 3.2. Such a global stability ensures the operation inside the sliding surface (12), i.e. $S_U = \{s_x = 0\}$. Therefore, the SMC imposes $i_{Cp} = -k \cdot (v_p - v_n)$, and replacing (6) and (9) leads to the equivalent dynamics in closed loop for the bus voltage. Since the desired operation condition is $v_p = v_n = v_b/2$, the resulting time-domain expression (18) is obtained by using $v_p - v_n = 2 \cdot v_p - v_b$. Then, (18) is transformed to Laplace domain as given in (19), which relates the perturbations of the positive bus voltage v_p with the desired condition $v_b/2$.

$$C_p \cdot \frac{d\, v_p}{dt} = -k \cdot (2 \cdot v_p - v_b) \quad (18)$$

$$G_{CL} = \frac{\widehat{v_p}}{(\widehat{v_b}/2)} = \frac{1}{\left(\frac{C_p}{2 \cdot k}\right) \cdot s + 1} \quad (19)$$

The design of k is performed for the worst-case scenario, which considers a step-change on the bus voltage equal to the maximum deviation allowed Δv_p. Such a perturbation is formalized, in Laplace domain, as $\widehat{v_b}/2 = \frac{\Delta v_p}{s}$. Then, the dynamic behavior of the bus voltage is calculated as $\widehat{v_p} = G_{CL} \cdot \frac{\Delta v_p}{s}$, which results in the time-domain expression for the bus voltage given in (20). The settling-time is measured when the bus voltage enters a safe ϵ band, i.e. $\widehat{v_p} = \epsilon \cdot v_b/2$, hence the voltage needed to compensate is $\Delta v_p - \epsilon \cdot v_b/2$. Thus, such a compensation value is replaced in (20) to obtain the design expression for k given in (21), which ensures the desired settling-time to the bus.

$$\widehat{v_p} = \Delta v_p \cdot \left(1 - e^{-t/\left(\frac{C_p}{2 \cdot k}\right)}\right) \quad (20)$$

$$k = \frac{-\ln\left(\frac{\epsilon \cdot v_b/2}{\Delta v_p}\right) \cdot C_p}{2 \cdot t_s} \quad (21)$$

3.4. Switching frequency

The theoretical sliding surface given in (12) could introduce very high switching frequencies near $s_x = 0$. This problem is commonly faced by introducing a hysteresis band around the surface [13], which limits the maximum switching frequency F. The formalization of such a limitation is reported in (22), where H is the hysteresis band.

$$S_{UP} = \{s_x \leq H\} \quad (22)$$

The previous practical surface imposes a ripple in the switching function equal to H. Such a ripple is calculated from (11) as $H = \Delta i_L/2$, where Δi_L is the inductor current ripple. That Δi_L ripple is divided by 2 because the half of the inductor current is processed by capacitor C_P as reported in (2), i.e. $i_{Cp} = i_L/2$. Then, the inductor current ripple is calculated from (1) as $\Delta i_L = v_p \cdot d \cdot T/(2 \cdot L)$. Moreover, from (9) it is calculated a duty cycle $d = 0.5$ for the desired operation condition $v_p = v_n = v_b/2$. Based on the previous analyses, it is calculated expression (23) for the hysteresis band H, which ensures a maximum switching frequency F.

$$H = \frac{v_p}{8 \cdot L \cdot F} \quad (23)$$

4. BUS CAPACITANCES DESIGN

The calculation of the bus capacitances $C_P = C_n$ is performed to limit the bus voltages deviation caused by the maximum current perturbation Δi_o allowed in the bipolar bus. This calculation requires the analysis of the current and voltage waveforms in the C_P capacitor. Fig. 2 shows the ground node of the bipolar charger/discharger, and the analysis considers a step-change on the bus current Δi_o, which is the worst-case scenario. The waveform of the output current i_o exhibits a step-down perturbation with magnitude Δi_o, which is compensated by the SMC with a decrement in the C_P capacitor current i_{Cp}. However, expression (2) reports that the capacitor current depends on the half of both output current i_o and inductor current i_L, thus the step in the load current Δi_o is instantaneously translated to i_{Cp} divided by 2. Instead, the inductor current can change with the maximum slope defined in (1), hence its effect is translated to i_{Cp}, divided by 2, during a time interval ΔT_Q. Fig. 2 shows those i_o, i_L and i_{Cp} waveforms.

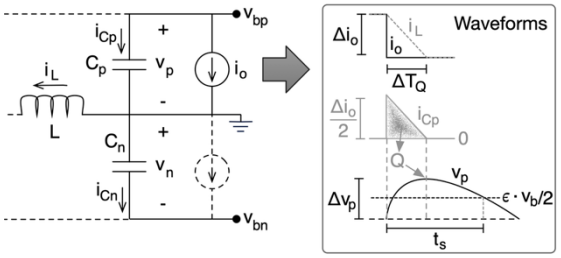

***Fig. 2**. Bus voltage deviation analysis.*
***Source:** own elaboration.*

The interval ΔT_Q is the time needed by i_{Cp} to reach 0 starting from $\Delta i_o/2$, resulting in expression (24). Such an expression uses the inductor current derivative reported in (1) for $u = 1$.

$$\Delta T_Q = \frac{\Delta i_o/2}{\frac{1}{2} \cdot \frac{d\, i_L}{dt}} = \frac{2 \cdot L \cdot \Delta i_o}{v_b} \quad (24)$$

The i_{Cp} waveform shows that a positive charge Q is stored into C_P capacitor during the transient, which is calculated as the area of the triangle formed by $\Delta i_o/2$ and ΔT_Q, resulting in $Q = \Delta T_Q \cdot \Delta i_o/4$. The middle waveform of Fig. 2 shows this concept. Moreover, such a positive charge produces an increment into the C_P capacitor voltage v_p defined by $\Delta v_p = Q/C_P$. Finally, operating the previous expressions, including (24), enables the calculation of C_P value that ensures a maximum deviation Δv_p:

$$C_P = \frac{L \cdot {\Delta i_o}^2}{2 \cdot v_b \cdot \Delta v_p} \tag{25}$$

5. DESIGN PROCEDURE AND APPLICATION EXAMPLE

This section synthesizes the design process, which is also illustrated with an application example.

5.1. Synthesis of the design process

The first step is to define the application requirements: battery voltage (v_b), synchronous bipolar voltages ($v_p = v_n = v_b/2$), maximum current derivative in the buses $\left|\frac{d\, i_o}{dt}\right|$, maximum amplitude of the load current perturbations (Δi_o), maximum voltage deviation in the buses (Δv_p), settling-time (t_s) for a given safety band (ϵ), and maximum switching frequency supported by the components (F).

The second step is to calculate the inductor L from (17) to ensure global stability. The third step is to calculate the bus capacitances $C_P = C_n$ from (25), which limits the bus voltages deviations to Δv_p. The fourth step is to calculate the weighting factor k from (21) to ensure the desired settling-time t_s. Finally, the hysteresis band of the SMC is calculated from (23) to limit the switching frequency up to F.

5.2. Application example

This application example considers a $v_b = 48\, V$ battery, which is used to support a synchronous bipolar bus providing $24\, V$ brances ($v_p = v_n = 24\, V$). In this example, the sources and loads connected to the bus impose a maximum current derivative in the buses $\left|\frac{d\, i_o}{dt}\right| = 100\, A/ms$, and with a maximum amplitude of the current perturbations $\Delta i_o = 2\, A$. Moreover, the correct operation of those sources and loads require to limit the branches' voltage deviations to 2.5 %, hence a maximum voltage deviation of $0.6\, V$ must be ensured. The loads and sources of this example support a voltage deviation during $t_s = 0.1\, ms$ for a band $\epsilon = 1\%$ $(0.24\, V)$ in the bus. Finally, the devices used in the converter's construction support a maximum switching frequency $F = 100\, kHz$. Those requirements for the application example are summarized in Table 1.

Table 1: *Requirements for the application example*

Requirement	Value
v_b	48 V
$v_p = v_n$	24 V
$\left\|\frac{d\, i_o}{dt}\right\|$	100 A/ms
Δi_o	2 A
Δv_p	2.5 % (0.6 V)
t_s	0.1 ms
ϵ	1% (0.24 V)
F	100 kHz

Source: *own elaboration.*

Then, following the design procedure of Subsection 5.1, a maximum converter inductance of $240\, \mu H$ is calculated from (17), where a commercial $L = 200\, \mu H$ is selected. The minimum bus capacitances $13.72\, \mu F$ are calculated from (25), selecting the commercial capacitors $C_P = C_n = 15\, \mu F$. Next, the weighting factor $k = 0.07\, A/V$ is calculated using (21). Finally, the hysteresis band $H = 0.15\, A$ is calculated from (23). Table 2 summarizes the parameters of the bipolar charger/discharger.

Table 2: *Parameters of the bipolar charger/discharger*

Parameter	Value
L	200 μH
$C_p = C_n$	15 μF
k	0.07 A/V
H	0.15 A

Source: *own elaboration.*

6. CIRCUITAL SIMULATIONS

The previous design example is verified using detailed circuital simulations performed in the professional power electronics simulator PSIM® 2022. The simulator was configured with a time-step of 10 ns, and the MOSFETs model includes an ON resistance of 4.8 mΩ, a diode forward voltage of 3 V, and a parasitic diode resistance of 1 mΩ.

Then, the circuital scheme of fig. 1 was implemented using the parameters of Table 2. Fig. 3

shows the PSIM circuit, where the voltage of the negative bus is measured at the lower node, thus it is the negative value of the bus voltage magnitude. This is compensated by adding both positive and negative bus voltages to form the component $k \cdot (v_p - v_n)$ of the function s_x (11).

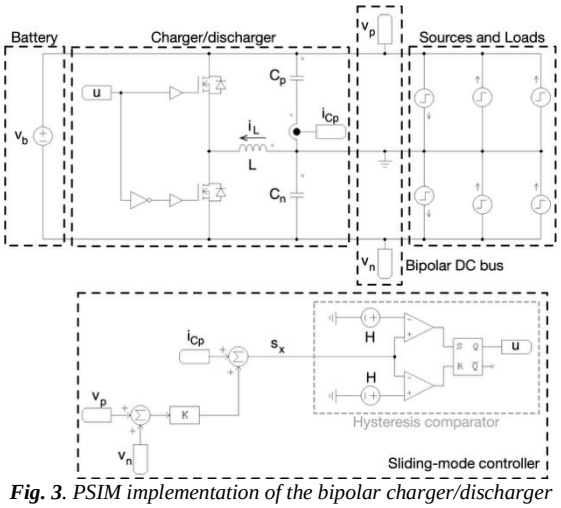

Fig. 3*. PSIM implementation of the bipolar charger/discharger*
Source: *own elaboration.*

In addition, fig. 3 also shows the hysteresis comparator implementing the practical sliding surface $S_{UP} = \{s_x \leq H\}$ previously defined in (22). Such a hysteresis comparator is formed by two classical comparators and a S-R flip-flop, which produces the control signal u of the MOSFETs.

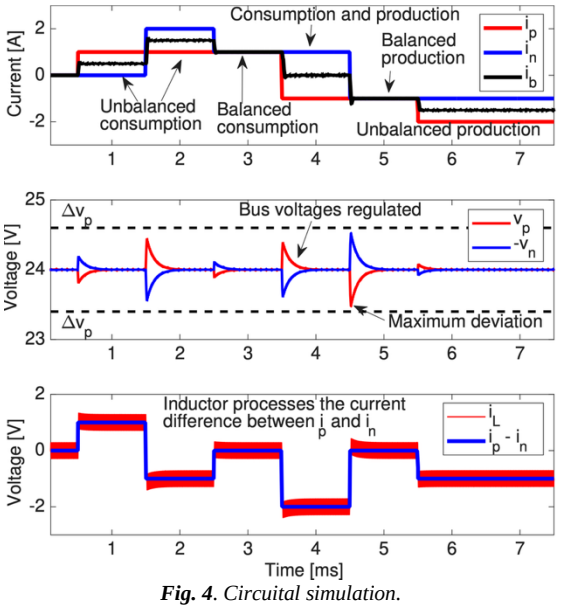

Fig. 4*. Circuital simulation.*
Source: *own elaboration.*

The simulation circuit of fig. 3 considers six current changes on both positive and negative buses. Fig. 4 reports the simulation results, where at 0.5 ms the positive bus has a current consumption of 1 A, which produces an unbalanced consumption since the negative bus is in stand-by (0 A). In such a condition both buses are perturbed, but they are correctly regulated; the voltage deviation in this case is small (0.8 %) since the current perturbation is smaller than the Δi_o defined in Table 1, fulfilling the voltage deviation requirement (lower than 2.5 %). At 1.5 ms the negative bus has a current perturbation of 2 A (equal to Δi_o in Table 1), thus producing an unbalanced consumption. Again, both bus voltages are perturbed and correctly regulated with a deviation of 1.9 % < 2.5 %. At 2.5 ms the current consumption in the negative bus is reduced to 1 A, which produces a balanced current consumption; again, both buses are regulated with a voltage deviation of 0.5 % < 2.5 %.

At 3.5 ms the current in the positive bus becomes negative (-1 A), which means that a source is producing energy. Therefore, in such a condition both consumption (negative bus) and production (positive bus) are occurring at the same time. As in the previous cases, both bus voltages are correctly regulated with a deviation of 1.7 % < 2.5 %. At 4.5 ms the current in the negative bus becomes negative, which means that a source in that bus is also producing energy. This generates a balanced production in both buses (-1 A), where a $\Delta i_o = 2\ A$ occurs (the same defined in Table 1). In this case both bus voltages are correctly regulated with a deviation of 2.2 % < 2.5 %. Finally, at 5.5 ms the production in the positive bus is increased (-2 A), hence generating an unbalanced production in the bipolar DC bus. As in the previous cases, both bus voltages are correctly regulated, in this case with a deviation of 0.4 % < 2.5 %. In conclusion, the circuital simulation of fig. 4 confirms the correct regulation of the bipolar DC bus in any operation condition. In addition, it is observed that the battery current is always the average value of the current in both buses. This is expected since a current production in one bus can be used to supply a current consumption in the other bus. This is confirmed in the bottom waveforms, where the inductor current only processes the difference between the currents in the buses.

Fig. 5 shows a zoom between 4.46 ms and 4.70 ms, which corresponds to the $\Delta i_o = -2\ A$ transient in the negative bus. The figure confirms the correct design of both the converter and the controller: the bus voltage deviation is always below the limit $\Delta v_p = 0.6\ V$ (0.53 V or 2.2 % < 2.5 %), and the settling time is equal to $t_s = 0.1\ ms$ for a band $\epsilon = 1\%$ $(0.24\ V)$. Finally, the switching frequency

(measured in i_L) is equal to 100 kHz. In conclusion, the proposed design process (resulting in the parameters of Table 2) provides the desired operation characteristics defined in Table 1.

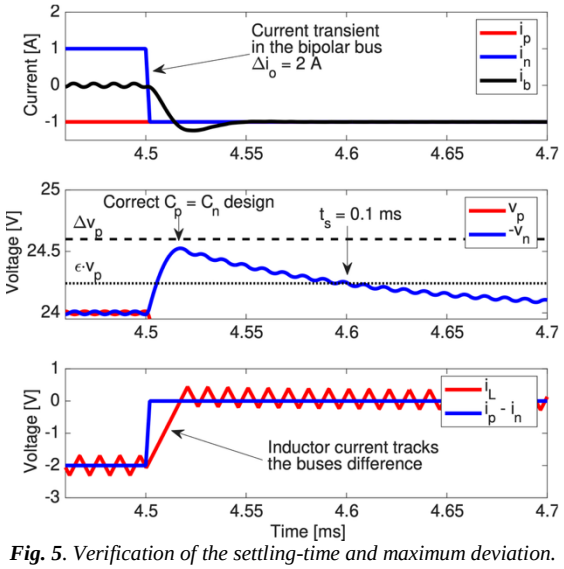

***Fig. 5**. Verification of the settling-time and maximum deviation.*
***Source:** own elaboration.*

7. CONCLUSIONS AND FUTURE WORK

This work has successfully proposed, designed, and verified a battery charger/discharger system tailored explicitly for synchronous bipolar DC microgrids. The core of the system is a sliding-mode control (SMC) strategy that effectively regulates the bipolar bus voltages, ensuring the positive (v_p) and negative (v_n) rails remain equal in magnitude and stable. The global stability of this non-linear controller was rigorously confirmed through transversality and reachability analyses, underscoring its robustness for switched converter applications. A significant contribution of this research is the establishment of a comprehensive, systematic design procedure that enables the calculation of critical parameters including the inductor (L), bus capacitances (C_p, C_n), the sliding-surface weighting factor (k), and the hysteresis band (H). Those calculations are based on the application requirements such as maximum voltage deviation, settling time, and maximum switching frequency.

The performance of the designed converter and its controller was validated through circuit simulations in PSIM under various operational scenarios, including both balanced and unbalanced conditions of current consumption and production. The results confirmed robust voltage regulation, meeting all desired operational characteristics. Furthermore, the system demonstrated efficient energy flow management, allowing current production in one bus to supply consumption in the other, as confirmed by the simulated battery current, which corresponds to the average value of the currents in both buses.

Based on these findings, several future works are proposed. The most immediate step is to experimentally validate this solution with a physical prototype, confirming the theoretical and simulation results under real-world conditions that account for practical non-idealities and component tolerances. Subsequently, research could focus on enhancing the system's fault tolerance by investigating its performance during anomalous conditions such as short circuits, open circuits in a bipolar branch, or extreme load transients. Those analyses will involve developing advanced fault detection and protection mechanisms. Finally, while the current control ensures stability, future work could explore optimization techniques to enhance overall efficiency and dynamic response, investigate alternative modulation techniques, utilize wide-bandgap (WBG) semiconductors, or develop adaptive control algorithms to minimize losses and improve transient performance across a broader range of operating points.

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