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Step Up/Down Rectifier with Power Factor Correction based on a Cuk converter and sliding-mode control

Rectificador Elevador/Reductor con Corrección de Factor de Potencia basado en un convertidor Cuk y control por modos deslizantes

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Abstract: The demand for reactive power from the distribution system and the production of current harmonics due to nonlinear active loads reduce the active power transport capacity, produce electrical losses and alter the voltage in the feeder buses of the distribution network. To face these challenges, this paper presents the design of a step-up/down rectifier and its control system to correct the power factor and mitigate the current harmonics produced by non-linear loads. The power interface is based on a Cuk converter, which enables to supply DC loads with voltages higher or lower than the peak value of the grid voltage. The Cuk converter is connected between the rectifier and the DC load. The main contribution of this work consists in a design method for the Cuk converter and its control system, ensuring specifications of the distribution system, the converter, and the load. The methodology consists of a design procedure of three controllers and the converter from their electrical and mathematical models. The design procedure is validated through two application examples simulated in the PSIM software. The results show the effectiveness of the design in mitigating harmonics, producing a power factor equal to one, maintaining low ripple and regulating the voltage at the load. The results show that the proposed design guarantees a ripple percentage in the grid of 2.5% and in the load of 5%, a power factor practically equal to unity, and voltage regulation in the expected number of cycles.

Keywords: Rectification, Power factor, Harmonic content, Cuk converter, Non-linear control.

Resumen: La demanda de potencia reactiva al sistema de distribución y la producción de armónicos de corriente debidas a las cargas activas no-lineales reducen la capacidad de transporte de potencia activa, producen pérdidas eléctricas y alteran el voltaje en los buses alimentadores de la red de distribución. Para hacer frente a estos retos, este artículo presenta

el diseño de un rectificador elevador/reductor y su sistema de control para corregir el factor de potencia y mitigar los armónicos de corriente producidos por las cargas no-lineales. La interfaz de potencia se basa en un convertidor Cuk, lo que permite atender cargas DC con voltajes mayores o menores al valor pico del voltaje rectificado de la red eléctrica. El convertidor Cuk se conecta entre un rectificador tradicional y la carga DC. La principal contribución de este trabajo consiste en un método de diseño del convertidor Cuk y su sistema de control, garantizando especificaciones del sistema de distribución, del convertidor y de la carga. La metodología consiste en un procedimiento de diseño de tres controladores y el convertidor a partir de sus modelos eléctrico y matemático. El procedimiento de diseño se valida a través de dos ejemplos de aplicación simulados en el software PSIM. Los resultados muestran la efectividad del diseño para mitigar armónicos, producir un factor de potencia igual a uno, mantener un bajo rizado y regular el voltaje en la carga. Específicamente, los resultados muestran que el diseño propuesto garantiza el porcentaje de rizado en la red de 2.5% y en la carga del 5%, el factor de potencia prácticamente igual a la unidad, y la regulación del voltaje en el número esperado de ciclos.

Palabras clave: Rectificación, Factor de potencia, Contenido armónico, Convertidor Cuk, Control no-lineal.

1. INTRODUCTION

High power quality is essential to ensure a safe and optimal operation of any electronic equipment, which reduces the overheating and power losses. A high-power quality is achieved when the instantaneous deviations of the system' voltage, in both magnitude and waveform, are into acceptable ranges for the electrical equipment. The main criteria to evaluate the power quality are the RMS value and frequency of the voltage, the waveform, the Total Harmonic Distortion (THD), the Power Factor (PF), fluctuations, interruptions, transients, noise, among others [1] [2] [3].

The PF is defined in terms of the relation between the real and apparent power magnitudes, or between the current and voltage waveforms if both signals are pure sine waves [3] [4]. Fig. 1 shows the simulation of a single-phase rectifier with an inductive load, where the PF measured between the active and apparent power is near 0.83, while the cosine between both current and voltage waveforms, which are not pure sine waves, is near 0.93. Therefore, the last value is wrong since the harmonic distortion is not considered.

The PF correction and harmonic reduction are regulated by the IEC 61000-3-2 standard [5], which defines the limit of harmonic content that can be injected into the grid. The PF correction is commonly a user responsibility, since the main causes of PF degradation are the user loads.

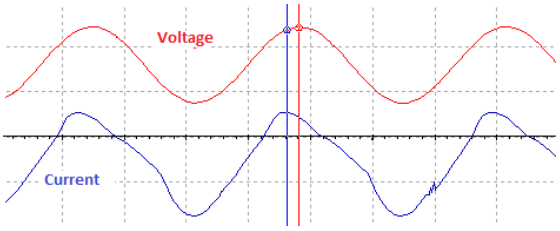

***Fig. 1**. Voltage and current characteristics at the input of a single-phase rectifier with an inductive load and no PF correction. **Source:** own elaboration.*

In this way, inductor loads such as motors, transformers and electronic ballast, equipment that produce harmonics such as frequency converters and non-linear loads, sub-compensation and over-compensation using capacitors, all those are the main reasons that force the grid generators to produce reactive power, also degrading the PF from the ideal unitary value. The consumption of reactive power does not produce useful work; hence the same active power consumption (with lower PF) increases the current consumption, which increases the energy losses due to the Joule effect, heating the equipment and increasing the operation costs due to the penalization imposed by grid providers [1].

In AC-DC power converters, the combination of the rectifier, the non-linear converter, and the capacitive filter generate a large distortion in the input (grid) current; this problem has been faced in two ways to improve the PF and reduce the THD. The first solution is to add an inductor,

which could be introduced between the rectifier and the capacitor, or in the AC side at the rectifier input. The combination of both solutions is usually more effective, where the inductor prevents strong changes on the current, hence the rectifier currents (input and output) are not discontinuous. This is a low-cost, simple and reliable method with low Electromagnetic Interference (EMI), but it has a large size, high weight, and difficult to provide a PF near to one.

The other solution is the active PF correctors, which is based on a switched DC/DC converter at the output of the rectifier. These circuits can reach near unitary PF, correct the THD and regulate the output voltage; however, this solution is more complex, has higher cost and can produce higher EMI [6] [7]. Likewise, many of those solutions are designed for specific applications, which makes difficult its adoption for other purposes. In particular, PF correctors are designed as step-up or step-down circuits depending on the application, hence no general design process has been found. This put into evidence a lack of generality in the power circuit, control system structure, and design process for rectifiers with PF correction, which can be applied to both step-up and step-down applications. The following literature review analyzes several PF correctors using switched converters to identify its characteristics.

In [8] is used a SEPIC converter to supply a LED load, which is regulated with an output voltage cascade controller based on a peak-current controller for the MOSFET. The PF correction is performed with the UC3842 integrated circuit, which forces the rectified current to follow the grid current, obtaining a PF higher than 0.9 for a current range between 50 mA and 300 mA at 100 Vdc. That circuit is a peak-current controller, but the additional outer voltage loop is not specified. On the other hand, the work in [9] presents four topologies based on boost converters with PF correction for supplying LED loads.

The topologies have complex structures and require multiple coupled inductors, capacitors and diodes to guarantee a low-crest factor. These converters use a PI current controller, producing a high current ripple, near to 20%. The work does not report the achieved PF, and the THD oscillates between 4% and 13% depending on the load voltage. The system reported in [10] uses a Cuk converter, which is operated in discontinuous conduction mode (DCM) to correct the PF at the rectifier output. Moreover, the solution in [10] requires an additional buck converter to regulate the output voltage, which uses a moth flame optimization algorithm to obtain the PI parameters.

In [11], like [8], it is adopted a SEPIC converter, but this time operating in DCM to perform the PF correction. The voltage controller adopted for the SEPIC is a classical PI, and the PF is corrected to 0.9. A variation of the boost converter, named quasi-resonant, with zero switching current to improve the PF, is presented in [12]. The closed-loop operation is performed using a classical PI controller for the output voltage. However, that work does not quantify the PF correction, and the design process of both power and control stages is not reported.

In [13] it is reported an AC-DC system with multiple rectifier cells, each one formed by two single-phase rectifiers and a non-controlled and isolated DC/DC converter. Those cells are connected to divide the input AC voltage, and the output is driven by a boost converter with a non-specified controller. Another work based on boost converter, but with an interleaved mode, is presented in [14]. Such a converter is connected the output of a rectifier, and it is controlled using classical PID controllers for both the current and voltage in cascade configuration; however, the controller design is not discussed. Finally, a PF near to 1 is achieved with a regulated output voltage. Another SEPIC solution, with sliding-mode control, is reported in [15], where the converter is described using a simplified second-order model that introduces a steady-state error at the output voltage. This converter is regulated with current and voltage sliding-mode controllers in cascade mode; however, the parameters selection for the converter and controllers is not analyzed.

The PF improvement of an AC-DC-AC system that feeds a Brush-less DC (BLDC) motor is reported in [16], which uses a LC filter followed by a non-isolated converter formed by a MOSFET, a diode, an inductor, a capacitor and a Fuzzy controller. The converter is operated in DCM, but the design of both the controller and power stage are not discussed. Another work based on a boost converter and a single-phase

rectifier is reported in [17], which in this case is regulated with an adaptive neuro-fuzzy voltage controller. That solution reaches a near 1 PF and improves the THD, but the work does not report the power stage design, where a single flowchart describes the control algorithm without any implementation details.

The wireless power transmission also requires PF correction as it is discussed in [18]. That system uses the traditional boost converter and a classical PI controller. In that way it is designed a current-loop that ensures a near one PF at the rectifier input, which feeds an inverter that produces the high-frequency signal for the wireless power transmission. Another system based on the UC3854 integrated circuit for PF regulation is reported in [19], where the boost topology is adopted to regulate the PF between 0.8 and 1.0. In this case, the current and voltage controllers are implemented in a FPGA, specifying its design and structure. Finally, it is required an additional synchronous buck converter to regulate the output voltage.

Another intelligent controller applied to the boost converter is reported in [20], where the voltage controller is based on fuzzy logic, and the current controller is based on a predictive structure. Using those cascade controllers, the PF is corrected. On the other hand, in [21] are used two switched converters, a boost and a buck, which are integrated to perform the PF correction and the output voltage regulation. In that solution the rectification process is performed by the boost converter, but the system is tested in open loop only.

The design and implementation of a sliding-mode control for a PF corrector, based on the boost converter, is reported in [22]. That system uses a linear controller for the voltage loop and a sliding-mode controller for the current loop, which ensures stability. Another application based on the boost converter, with a zero-voltage switching (ZVS), is discussed in [23]. That solution uses a controller based on the integrated circuit TL431, but any detail about the configuration is given. Finally, the PF is always over 0.9 for different load conditions.

It is clear the large use of the boost converter for active PF correction. However, the boost-only characteristic constrains this corrector to applications in which the output DC voltage is higher than the peak voltage of the rectifier. Other approaches use SEPIC or Cuk converters to provide lower voltages for LED lamps, but a general design procedure is not discussed. In terms of control, there is a large adoption of PI controllers due to its simplicity, but more complex approaches based on sliding-mode ensure global stability, which is not possible with linear (PI, PID) controllers.

This paper aims to provide a general solution for voltage rectification with PF correction. The power stage is based on the Cuk converter, where its input inductor regulates the rectifier current, and its output inductor reduces the harmonic injection into the DC load. The control system is based on sliding-mode control to provide a global stability for any DC voltage condition, even near zero current. Moreover, both the Cuk converter and sliding-mode controller enable to supply DC voltages higher or lower than the peak grid voltage, thus supporting step-up and step-down applications. Finally, a systematic design method is proposed, which ensures that application requirements are fulfilled.

The paper is organized as follows: the mathematical model is presented first, then the current controller, the PF correction and the voltage controller are discussed. Subsequently, the converter parameters are calculated, and a summary of the design process is reported. Finally, the results discussion and conclusions are given.

2. ELECTRICAL AND MATHEMATICAL MODELS

The electrical scheme of the rectifier with PF correction, based on the Cuk converter, is depicted in Fig. 2. The circuit uses a full-bridge rectifier to connect the AC grid with the Cuk converter, which imposes a unipolar voltage v_{rec} at the input of the converter. The output of the Cuk converter is connected to the load, which impedance is modeled as Z_{dc}.

The scheme also describes the control system blocks: first there is a current control, which defines the inductor L_1 current to regulate the rectifier current; second, there is a PF correction strategy, which defines the reference current i_r for the current control; finally, there is a load voltage

controller, which defines the peak value i_{pk} of the current imposed to the rectifier using L_1.

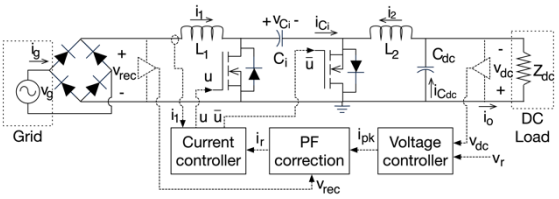

***Fig. 2**. Rectifier based on the Cuk converter with voltage regulation and PF correction.*
***Source:** own elaboration.*

The differential equations for the inductor currents (i_1 for L_1 and i_2 for L_2) are reported in (1) and (2) for the condition u = 1 of the control signal. Similarly, the differential equations for the intermediate capacitor C_i voltage (v_{Ci}) and output capacitor C_{dc} voltage (v_{dc}) are reported in (3) and (4).

$$\frac{di_1}{dt} = \frac{v_{rec}}{L_1} \quad (1)$$

$$\frac{di_2}{dt} = \frac{-v_{dc} + v_{Ci}}{L_2} \quad (2)$$

$$\frac{dv_{Ci}}{dt} = \frac{-i_2}{C_1} \quad (3)$$

$$\frac{dv_{dc}}{dt} = \frac{i_{2i} - v_{dc}/Z_{dc}}{C_1} \quad (4)$$

The differential equations for the inductor currents and capacitor voltages, for u = 0 condition, are reported in (5) – (8):

$$\frac{di_1}{dt} = \frac{v_{rec} - v_{Ci}}{L_1} \quad (5)$$

$$\frac{di_2}{dt} = \frac{-v_{dc}}{L_2} \quad (6)$$

$$\frac{dv_{Ci}}{dt} = \frac{i_1}{C_1} \quad (7)$$

$$\frac{dv_{dc}}{dt} = \frac{i_{2i} - v_{dc}/Z_{dc}}{C_1} \quad (8)$$

Combining the differential equations for both possible conditions of the control signal (u = 1 and u = 0) leads to the switched mode of the system:

$$\frac{di_1}{dt} = \frac{v_{rec} - v_{Ci} \cdot \bar{u}}{L_1} \quad (9)$$

$$\frac{di_2}{dt} = \frac{-v_{dc} + v_{Ci} \cdot u}{L_2} \quad (10)$$

$$\frac{dv_{Ci}}{dt} = \frac{-i_2 \cdot u + i_1 \cdot \bar{u}}{C_1} \quad (11)$$

$$\frac{dv_{dc}}{dt} = \frac{i_{2i} - v_{dc}/Z_{dc}}{C_1} \quad (12)$$

The average value of the control signal u within the switching period T_{sw} is equal to the duty cycle of the converter, as it is described in (13). Therefore, the averaged model of the power system is:

$$d = \int_o^{T_{sw}} u \, dt \quad (13)$$

$$\frac{di_1}{dt} = \frac{v_{rec} - v_{Ci} \cdot (1-d)}{L_1} \quad (14)$$

$$\frac{di_2}{dt} = \frac{-v_{dc} + v_{Ci} \cdot d}{L_2} \quad (15)$$

$$\frac{dv_{Ci}}{dt} = \frac{-i_2 \cdot d + i_1 \cdot (1-d)}{C_1} \quad (16)$$

$$\frac{dv_{dc}}{dt} = \frac{i_2 - v_{dc}/Z_{dc}}{C_1} \quad (17)$$

The electrical relation in steady state are obtained from the averaged model with null derivatives, leading from the following equations:

$$v_{rec} = v_{Ci} \cdot (1-d) \quad (18)$$

$$v_{dc} = v_{Ci} \cdot d \quad (19)$$

$$i_2 \cdot d = i_1 \cdot (1-d) \quad (20)$$

$$i_2 = i_o = v_{dc}/Z_{dc} \quad (21)$$

3. SOLUTION METHODOLOGY

The design of the rectification system has four stages: the current controller design, the power factor correction, the voltage controller design, and the converter elements design.

3.1. Current controller

The current control is performed with the sliding-mode technique, which is robust to parametric variations, operates with binary control signals, and ensures the global stability in non-linear systems [24]; those characteristics make ideal this technique for power electronics control.

The sliding-mode control (SMC) requires defining a switching function S_x to impose the desired behavior, which is ensured by forcing the switching function to be within the sliding surface $S_x = 0$. Considering that the current controller

regulates the rectifier current, which is equal to i_1, the switching function S_x and the sliding surface are defined as given in (22). Moreover, the derivative of S_x is given in (23), which is used in the stability analyses.

$$S_x = \{i_1 - i_r\} \wedge S_x = 0 \tag{22}$$

$$\frac{dS_x}{dt} = \frac{v_{rec} - v_{Ci} \cdot \bar{u}}{L_1} \tag{23}$$

The stability analysis of the SMC for power converters requires the evaluation of tree criteria [24]: transversality condition, reachability condition and equivalent control condition.

3.1.1. Transversality condition

The transversality condition evaluates the presence of the control signal (u) within the switching function derivative, which enables to modify the system trajectory. This condition is formalized as:

$$\frac{d}{du}\left(\frac{dS_x}{dt}\right) \neq 0 \tag{24}$$

Evaluating (24) with the S_x derivative reported in (23) confirms the transversality condition:

$$\frac{d}{du}\left(\frac{dS_x}{dt}\right) = \frac{v_{Ci}}{L_1} > 0 \tag{25}$$

On the other hand, the sign of the transversality value provides information about the effect of the control signal (u) on the derivative of S_x:

- Positive value: a positive change on u (0 to 1) produces a positive S_x derivative, and a negative change on u (1 to 0) produces a negative S_x derivative, i.e. direct action.
- Negative value: a positive change on u (0 to 1) produces a negative S_x derivative, and a negative change on u (1 to 0) produces a positive S_x derivative, i.e. inverse action.

Therefore, in this case, the SMC based in (22) has a direct action.

3.1.2. Reachability condition

The reachability condition evaluates the SMC capacity to reach the sliding-surface $S_x = 0$ from any operation condition. This is analyzed as follows:

- When the system operates under the surface ($S_x < 0$), the S_x derivative must be positive to reach the surface $S_x = 0$. Considering the direct action of the system, this is formalized as:

$$\lim_{S_x \to 0^-} \frac{dS_x}{dt}\bigg|_{u=1} > 0 \tag{26}$$

- When the system operates above the surface ($S_x > 0$), the S_x derivative must be negative to reach the surface $S_x = 0$:

$$\lim_{S_x \to 0^+} \frac{dS_x}{dt}\bigg|_{u=0} < 0 \tag{27}$$

Evaluating (26) and (27) with the S_x derivative given in (23) confirms that both reachability conditions are fulfilled:

$$\left\{ \begin{array}{c} \lim_{S_x \to 0^-} \frac{dS_x}{dt}\Big|_{u=1} = \frac{v_{rec}}{L_1} > 0 \\ \lim_{S_x \to 0^+} \frac{dS_x}{dt}\Big|_{u=0} = \frac{v_{rec} - v_{Ci}}{L_1} < 0 \end{array} \right\} \tag{28}$$

3.1.3. Equivalent control condition

The equivalent control condition evaluates if the average value u_{eq} of the control signal u is constrained by the values of u. For switching converters, the values of u are 1 and 0, and the average value of u is equal to the duty cycle (13). Therefore, the equivalent control condition evaluates the saturation of the duty cycle:

$$0 < u_{eq} = d < 1 \tag{29}$$

Sira-Ramírez demonstrated in [24] that a SMC fulfilling both transversality and reachability conditions also fulfills the equivalent control condition. Hence, the SMC based on (22) is globally stable because the control variable defines the system' trajectory (transversality), the system reaches the surface $S_x = 0$ from any operation point (reachability), and after entering the surface it never leaves it (equivalent control). Finally, the SMC stability is ensuring that $S_x = 0$ in any condition, hence $i_1 = i_r$. Therefore, the rectifier current is defined by i_r.

3.2. Power factor correction

The power factor correction is executed by defining the rectifier current waveform to be equal to the rectifier voltage waveform; this forces both grid current (i_g) and voltage (v_g) waveforms to be equal and in phase, thus ensuring a power factor near to one.

The procedure for PF correction is illustrated in Fig. 3, where the rectifier voltage waveform (v_{rec}) is obtained by normalizing v_{rec} with respect to the grid peak value (v_{pk}). The amplitude of the current waveform is defined by the voltage controller, which is discussed in Subsection 3.3. The diagram in Fig. 3 considers the Cuk converter under the action of the current SMC, hence the converter behavior is represented using two current sources; the first one models the current control $i_1 = i_r$, and the second one models $i_2 = i_1 \cdot (1\text{-}d)/d = i_r \cdot (1\text{-}d)/d$ defined by the stable relation (20).

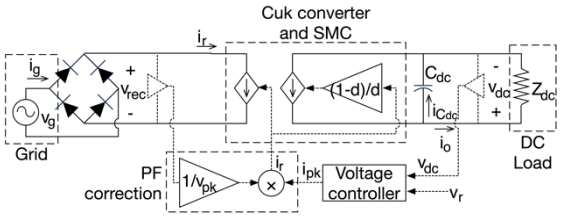

***Fig. 3**. Rectifier considering the action of the SMC and the PF correction strategy.*
***Source:** own elaboration.*

The i_r current waveform imposed by the PF corrector is given in (30), which corresponds to a sine waveform with amplitude i_{pk} and an AC grid frequency equal to f_g. Hence a unitary PF is ensured.

$$i_r = i_{pk} \cdot \left|\sin\left(2 \cdot \pi \cdot f_g \cdot t\right)\right| \tag{30}$$

The average value of i_r and v_{rec}, within the switching period, are given in (31) and (32), respectively, where v_{pk} is the AC grid peak value.

$$\langle i_r \rangle = \int_o^{T_{sw}} i_r \, dt = \frac{2 \cdot i_{pk}}{\pi} \tag{31}$$

$$\langle v_{rec} \rangle = \int_o^{T_{sw}} v_{rec} \, dt = \frac{2 \cdot v_{pk}}{\pi} \tag{32}$$

Finally, the PF corrector imposes an average duty cycle (within the switching period), calculated from (18), (19) and (32), equal to:

$$\langle d \rangle = \frac{v_{dc} \cdot \pi}{v_{dc} \cdot \pi + 2 \cdot v_{pk}} \tag{33}$$

3.3. Output capacitor C_{dc} and voltage control

The voltage oscillation at the DC output (v_{dc}), named Δv_{dc}, is calculated from the load current i_o and the output capacitance C_{dc}. The design equation of C_{dc} is discussed in [25], providing (34), where $\epsilon_{dc} = \Delta v_{dc}/v_{dc}$ is the acceptable ripple percentage at the DC output, i.e. at the load voltage:

$$C_{dc} = \frac{i_o}{4 \cdot \pi \cdot f_g \cdot \epsilon_{dc} \cdot v_{dc}} \tag{34}$$

From the model in Fig. 3 is obtained an output current of the Cuk converter equal to $i_r \cdot (1 - \langle d \rangle)/\langle d \rangle$, which leads to the following transfer function between the output DC voltage (v_{dc}) and reference current (i_r):

$$\frac{v_{dc}}{i_r} = \frac{Z_{dc}}{Z_{dc} \cdot C_{dc} \cdot s + 1} \tag{35}$$

Considering the average i_r value given in (31), the average duty cycle given in (33), and the relation $Z_{dc} = v_{dc}/i_o$ obtained from Fig. 3, equation (35) is modified to obtain the transfer function between v_{dc} and i_{pk} reported in (36).

$$G_{dc} = \frac{v_{dc}}{i_{pk}} = \frac{\left(\frac{4 \cdot v_{pk}}{\pi^2 \cdot i_o}\right)}{\frac{s}{4 \cdot \pi \cdot f_g \cdot \epsilon_{dc}} + 1} \tag{36}$$

The transfer function G_{dc} does not depend on the DC voltage imposed to the load, it only depends on the AC grid characteristics (v_{pk} and f_g), the acceptable ripple percentage, and the maximum load consumption. Finally, G_{dc} must be parameterized using the application data for designing the voltage controller, e.g. a PI structure, with a bandwidth lower than the grid frequency.

3.4. Switching frequency, inductors and intermediate capacitor C_i design

The SMC does not have a switching frequency limitation, which makes impossible the implementation with real MOSFETs. This is

solved by introducing a hysteresis band into the sliding-surface, which limits the maximum switching frequency [24]. Therefore, the sliding-surface defined in (22) is implemented with an additional hysteresis band [-ΔSx, +ΔSx]:

$$-\Delta S_x \leq S_x \leq +\Delta S_x \tag{37}$$

Since the switching function is $S_x = i_1 - i_r$, and i_r is a ripple-free signal, then the switching ripple in i_1 (Δi_1) is equal to the hysteresis band limit ($\Delta S_x = \Delta i_1$).

The switching ripple in i_1 is calculated from equation (1) for the interval $d \cdot T_{sw}$, where the maximum amplitude Δi_1 is obtained for the peak value of v_{rec}, i.e. $v_{rec} = v_{pk}$. Moreover, the instantaneous duty cycle for such a maximum condition is $d_{pk} = v_{dc}/(v_{dc}+v_{pk})$. Considering the previous conditions, and defining the switching frequency as $F_{sw} = 1/T_{sw}$, the amplitude Δi_1 is:

$$\Delta i_1 = \frac{v_{dc} \cdot v_{pk}}{2 \cdot L_1 \cdot F_{sw} \cdot (v_{pk} + v_{dc})} \tag{38}$$

To limit the THD introduced to the grid, the ripple $\Delta S_x = \Delta i_1$ is defined as a percentage $\epsilon_{i1} = \Delta i_1 / i_{pk}$ of the rectifier' peak current. In [25] was calculated the output current of a rectifier as $i_o = v_{pk} \cdot i_{pk}/(2 \cdot v_{dc})$, which leads to the hysteresis band calculated in (39), where ϵ_{i1} is defined to reach the desired THD, e.g. ϵ_{i1} = 2.5% (peak-to-peak ripple of 5%).

$$\Delta S_x = \Delta i_1 = \epsilon_{i1} \cdot \frac{2 \cdot v_{dc} \cdot i_o}{v_{pk}} \tag{39}$$

From equation (38) and considering the value $\Delta S_x = \Delta i_1$ calculated in (39), the inductor L_1 is calculated as given in (40) to impose the maximum F_{sw} value.

$$L_1 = \frac{v_{dc} \cdot v_{pk}}{2 \cdot \Delta S_x \cdot F_{sw} \cdot (v_{pk} + v_{dc})} \tag{40}$$

Equation (11) shows that the current in the intermediate capacitor C_i depends on i_1 and i_2. Therefore, the design of L_2 is performed to impose a current ripple balance on C_i. The current ripple on L_2 (Δi_2) is calculated from equation (6) for the interval $(1-d) \cdot T_{sw}$, and applying the same considerations made for L_1, the condition $\Delta i_2 = \Delta i_1$ requires $L_2 = L_1$ to obtain a ripple balance in C_i. The switching ripple in C_i is calculated from equation (3) for the time interval $d \cdot T_{sw}$, where the maximum amplitude Δv_{Ci} is obtained for the peak value v_{rec}. This design is performed in terms of the percentage ripple $\epsilon_{Ci} = \Delta v_{Ci}/v_{Ci}$, where the peak value $v_{Ci} = v_{dc} + v_{pk}$ is calculated from (19). Applying the same conditions adopted for the previous elements, and considering that the average value of i_2 is i_o as reported in (21), the value of C_i to ensure the desired ripple is:

$$C_i = \frac{i_o \cdot v_{dc}}{\epsilon_{Ci} \cdot F_{sw} \cdot (v_{pk} + v_{dc})^2} \tag{41}$$

3.5. Synthesis of the design process

The design process is summarized as follows:

1. Define the application requirements: peak voltage and AC grid frequency (v_{pk} and f_g), acceptable current ripple of the AC grid (ϵ_{i1}), DC voltage (v_{dc}), acceptable DC voltage ripple (ϵ_{dc}), maximum load current (i_o), maximum ripple in C_i (ϵ_{Ci}), maximum switching frequency (F_{sw}).
2. Calculate ΔS_x using (39).
3. Calculate L_1 using (40) and $L_2 = L_1$.
4. Calculate C_i using (41).
5. Calculate C_{dc} using (34).
6. Calculate transfer function G_{dc} using (36).
7. Design the voltage controller G_{cv} using G_{dc}, e.g. a PI structure with a bandwidth lower than the grid frequency.

4. RESULTS AND DISCUSSION

The verification of the proposed design and control process for the Cuk-based rectifier is performed with two study cases, the first one in boost mode and the second one in buck mode. The design criteria for both cases are reported in Table 1, where the AC grid has 120 V RMS, and the DC load has a maximum consumption of 1 A. The current ripple is defined as 2.5 % to limit the THD injected to the grid, and the voltage ripples are limited to 5 %, which ensures a high-power quality for the load. Moreover, the regulation time for the DC voltage (t_s) is limited to five grid cycles, and the control system is limited to one fifth of the grid frequency.

Table 1: *General criteria for the study cases*

Criteria	Symbol	Value
Grid peak voltage	V_{pk}	169.7 V (120 V RMS)
Grid frequency	f_g	60 Hz
Maximum switching frequency	F_{sw}	50 kHz
Maximum load current	i_o	1 A
Grid ripple percentage	ϵ_{i1}	2.5 %
DC ripple percentage	ϵ_{dc}	5%
C_i ripple percentage	ϵ_{Ci}	5%
Stabilization time of v_{dc}	t_s	$5/f_g$ = 83.33 ms
Bandwidth of the v_{dc} controller	BW	$f_g/5$ = 12 Hz

Source: *own elaboration.*

The first study case (boost mode) considers a DC voltage v_{dc} = 340 V, and the second study case (buck mode) considers v_{dc} = 85 V. After applying the procedure reported in Section 3.5 results in the parameters reported in Table 2. In must be noted that the hysteresis band is reduced when the DC voltage is decreased, which keeps the limit of the harmonic distortion in relation with the reduction of the grid peak current. Moreover, it is observed an increment in the inductors to provide the same switching frequency.

On the other hand, the value of the intermediate capacitor is almost constant, which is caused by the balance of the inductor current ripples. On the contrary, the output capacitor is increased to keep the voltage ripple relation in response to the reduction of the DC voltage. Finally, as it was anticipated in Section 3.3, the transfer function to design the voltage controller (G_{dc}) is the same. For implementation purposes, inductor L_1 must support the rectified grid voltage and current, while inductor L_2 must support the DC voltage and current; capacitor C_i must support the grid voltage divided by 1-d and both inductor currents, and C_{dc} supports the DC voltage and the current transients. Finally, the MOSFETs must support the inductor currents.

Table 2: *Parameters calculated from the study cases*

Parameter	Symbol	Case 1	Case 2
DC voltage	v_{dc}	340 V	85 V
Hysteresis band	ΔS_x	100 mA	25 mA
Inductors	L_1, L_2	11.3 mH	22.6 mH
Intermediate capacitor	C_i	523.5 nF	524.1 nF
Output capacitor	C_o	78.1 µF	312.1 µF
Transfer function to design the voltage controller	G_{dc}	$\frac{68.78}{0.02653 \cdot s + 1}$	
Voltage controller	G_{dc}	$\frac{0.015 \cdot (s + 100)}{s}$	

Source: *own elaboration.*

The voltage controller G_{cv} was designed with a PI structure, using the *sisotool()* from Matlab, which imposes a settling time equal to 83.33 ms and a bandwidth equal to 12 Hz; depending on the application, the controller structure and the design criteria can be modified. In any case, since the G_{dc} transfer function is the same, the same G_{cv} controller is used to regulate the DC voltage in both study cases; such a controller can be used to regulate any DC load voltage if the current consumption i_o is the same, otherwise the G_{dc} transfer function changes, and the controller G_{cv} must be modified.

The validation of those designs was performed using detailed simulations carried out in the power electronics simulator PSIM; fig. 4 shows the electrical scheme implemented in the simulator. The circuit describes the current SMC implementation and the PF correction: the SMC is implemented with am hysteresis comparator formed by two classical comparators and S-R flip-flop; moreover, it includes an adder that can be implemented with operational amplifiers. The PF correction uses a voltage sensor with gain 1/169.7, which can be implemented with operational amplifiers. Finally, the current waveform is imposed with an analog multiplier, which is available as integrated circuit, e.g. [26].

The voltage controller uses a differential voltage sensor implemented with operational amplifiers, a subtractor and a PI circuit, which are also implemented with operational amplifiers. Finally, the circuit considers the load as a Norton equivalent, which enables to simulate changes on the load.

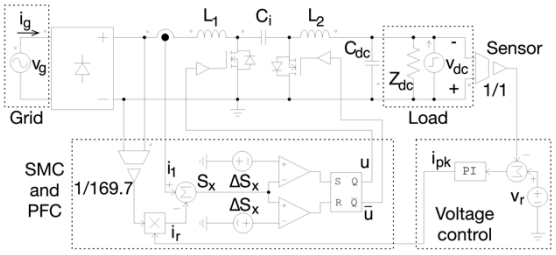

Fig. 4*. Electrical scheme for the detailed simulation in PSIM.*
Source: *own elaboration.*

The simulation results of Case 1 (boost mode) are reported in Fig. 5, where the average value of the load voltage (v_{dc}) is regulated at 340 V, and the voltage ripple for the maximum load consumption (1 A) is 5 % (17 V), which agrees with Table 1. The simulation considers a change

on the load current equal to 50 % (from 0.68 A to 1.02 A), where the correct regulation of v_{dc} is observed, and the stabilization time agrees with Table 1 (5 grid cycles, i.e. 83.33 ms). Finally, the simulation also shows the AC grid current and voltage, where the current is amplified 20 times to enable its visual comparison with the voltage. The PSIM software calculated the PF and THD: the PF is very near to one (0.9987) and the THD is low (4.19 %), which confirms the desired PF correction and the accurate voltage regulation at the load for boost conditions.

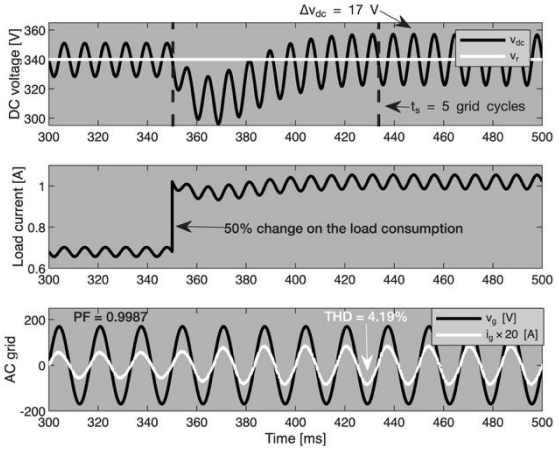

***Fig. 5**. Detailed simulation of the Cuk rectifier for Case 1 (boost mode, v_{dc} = 340 V). **Source:** own elaboration.*

The simulation results for Case 2 (buck mode) are reported in Fig. 6, where the average value of v_{dc} is correctly regulated at 85 V, and the voltage ripple for the maximum current consumption (1 A) is 5 % (4.25 V) as defined in Table 1. Like Case 1, the load has a 50 % change (from 0.68 A to 1.02 A), while the voltage controller ensures the same stabilization time (5 grid cycles), thus fulfilling the criterion define in Table 1. In this case the grid current is amplified 80 times to enable a visual comparison with the voltage, and the PSIM software reports a PF equal to Case 1 (0.9987) and a THD = 3.89 %, which confirms the power factor correction and the load voltage regulation for buck conditions.

The simulation results for Cases 1 and 2 confirm the correct performance of the design and control processes proposed for the Cuk rectifier, in both boost and buck modes. Therefore, the proposed procedure is a general solution to design rectifiers with power factor correction for any output voltage. Moreover, the simulations confirm the operation with low distortion in the AC side, and without a power factor degradation.

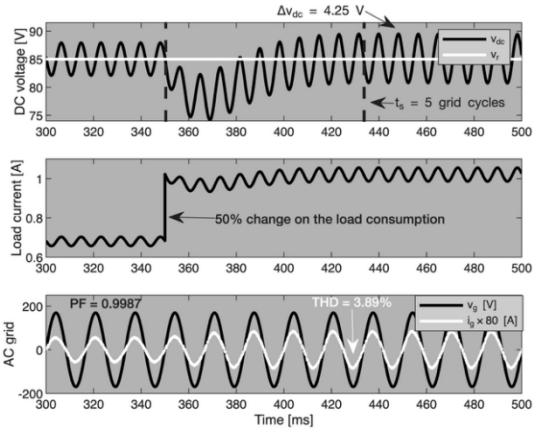

***Fig. 6**. Detailed simulation of the Cuk rectifier for Case 2 (buck mode, v_{dc} = 85 V). **Source:** own elaboration.*

With the aim of providing a comparison with other solutions, some commercial circuits were analyzed. For example, the UCC28064A integrated circuit [27] provides both power factor correction and voltage regulation. However, such a circuit is based on a boost converter topology, hence it cannot provide step-down rectified voltages. Similarly, the LM3447 integrated circuit [28] also provides PF correction, and it is based on a flyback topology.

However, this integrated circuit is designed for phase-cut dimmer LED lamp drivers, hence the turn-ratio of its transformer is defined for step-down conditions, and the control system is tuned for LED drivers' requirements. Moreover, the controller details for both UCC28064A and LM3447 integrated circuits, as it is for many commercial solutions, are not disclosed by the manufacturers; thus, its exact replication is not possible, and its adjustment to other applications is difficult. Therefore, both UCC28064A and LM3447 integrated circuits do not provide general solutions for step-up/down rectifiers with PF correction.

Then, the performance comparison considers a classical PI solution. To provide a fair comparison, the voltage controller is considered equal to the one defined in Table 2, thus ensuring the same settling-time (5 grid cycles). The PI controller for the i_1 current is designed by formulating a linearized small-signal model using the averaged equations (14)-(17); this linearization is performed for Case 1 (boost mode, v_{dc} = 340 V). Then, such a linear model is

used to calculate the C_{PI} controller given in (42), which imposes a closed-loop bandwidth of 1/5 of the switching frequency. This is the highest bandwidth achievable with a linear model, otherwise the controller will introduce over-modulation, thus increasing the current THD.

$$C_{PI} = \frac{0.27 \cdot (s + 10000)}{s} \tag{42}$$

Figure 7 reports the simulation results, where the average value of v_{dc} is regulated at 340 V, and the voltage ripple is 5 % (17 V), which agrees with Table 1. As in the previous simulations, this test considers a change on the load current equal to 50 %, where the correct regulation of v_{dc} is observed. In this case, the PF is acceptable and near to the proposed PFC solution (0.9980); however, the THD is 5.06 %, which is 20.8 % higher than the THD provided by the proposed PFC (reported in Figure 5). In addition, the THD of this PI solution does not fulfill the THD limit recommended by the IEEE Std. 2800-2022 (5 %) [29].

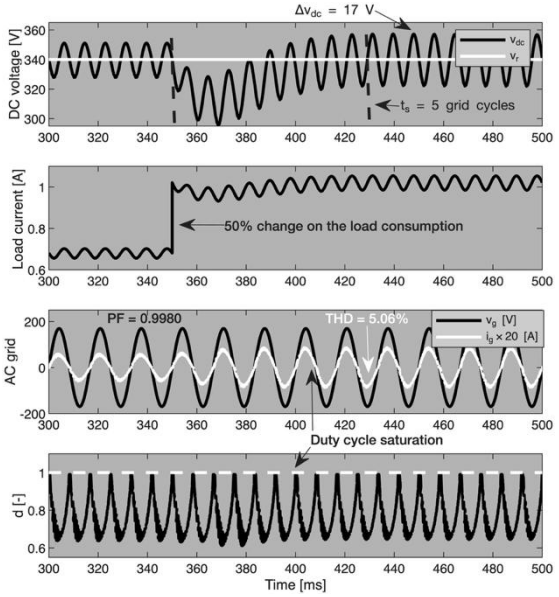

Fig. 7*. Detailed simulation of the Cuk rectifier for Case 1 with a PI current controller.*
Source: *own elaboration.*

Such a large THD condition is caused by the duty cycle saturation introduced by the PI controller near 0 V. This is the result of operating far from the linearization operation point, which cannot be avoided since the grid voltage must exhibit values near to zero and near to the peak value. Finally, changing the DC voltage to 85 V, or any other value, will require to recalculate the linearized model, thus the current controller given in (42) must be designed again. This is not needed with the proposed solution, since both current and voltage controllers are general for any DC voltage.

5. CONCLUSIONS

This paper has presented the design of a step up/down rectifier, based on the Cuk converter, and the control system to correct the power factor and mitigate the current harmonics produced by non-linear loads. The application example has demonstrated the design effectiveness to ensure the desired ripples in the grid, load and converter intermediate capacitor.

The design also demonstrated the solution effectiveness to produce a near unity power factor, regulating the output voltage with the desired number of grid cycles after a load change of 50 %, and mitigating the current harmonics.

The system has been tested with load voltages higher (340 v_{dc}) and lower (85 v_{dc}) than the peak voltage of the AC grid (120 v_{rms}), this thanks to the Cuk converter capacity and the correct design of the control system. Since the electric validation performed with PSIM guarantee the obtained results, it is possible to continue this research with the experimental design and implementation of the step up/down rectifier with power factor correction.

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